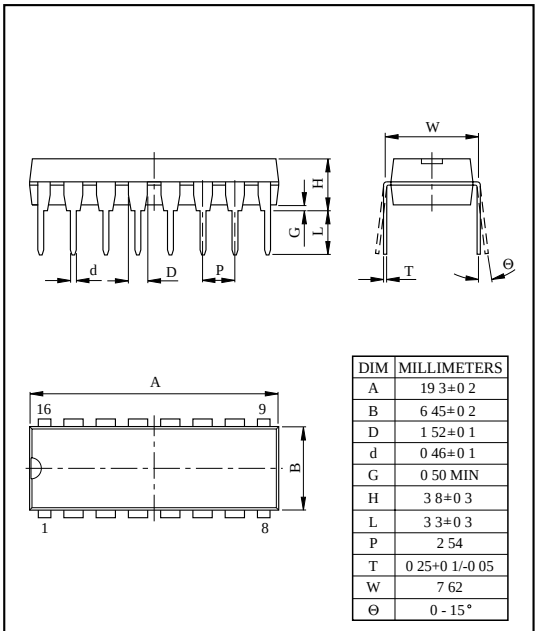
7 CIRCUIT DARLINGTON TRANSISTOR ARRAY

FEATURES

· Output Current : 500mA Max.
· High Sustaining Voltage Outputs : 50V Min.
· Output Clamp Diodes.
· Input Resistor : 2.7KΩ
· Inputs Compatible With TTL or 5V CMOS devices.
· PKG Type AP : DIP-16Pin, AF : FLP-16Pin



DIM	MILLIMETERS
A	19 3±0 2
B	6 45±0 2
D	1 52±0 1
d	0 46±0 1
G	0 50 MIN
H	3 8±0 3
L	3 3±0 3
P	2 54
T	0 25+0 1/-0 05
W	7 62
Θ	0 - 15°

DIP-16

DESCRIPTION:

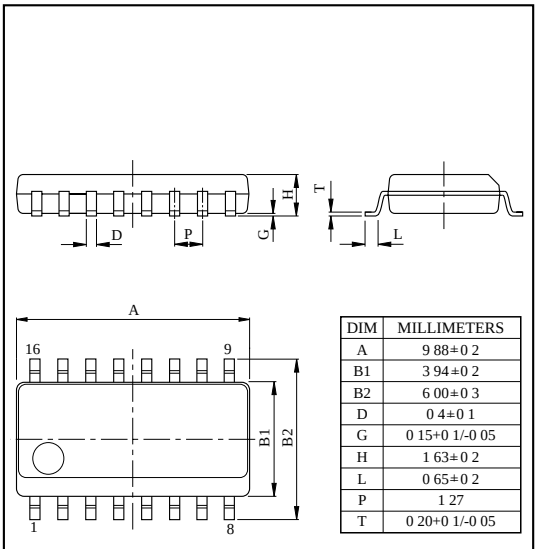
The FD62003AP/AF are high-voltage, high-current darlington transistor array comprised of seven NPN darlington pairs. All units feature internal clamp diodes for switching inductive loads.

APPLICATION :

· Relay Driver.
· Hammer Driver.
· Lamp and LED Display Driver.
· Line driver and Logic buffer.

MAXIMUM RATINGS (Ta=25℃, unless otherwise noted)

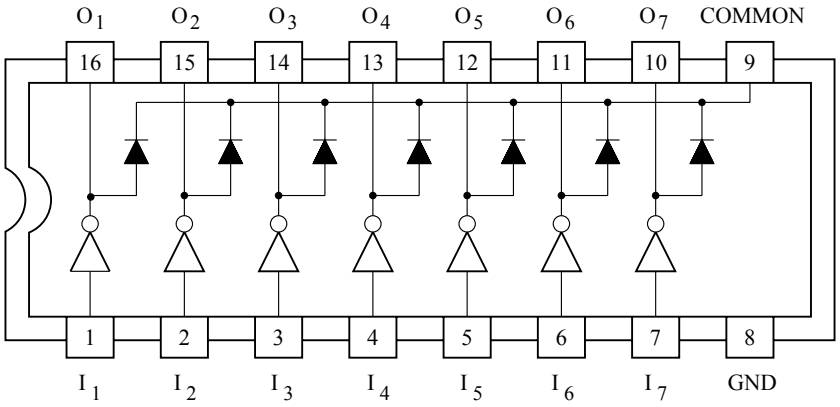
CHARACTERISTIC		SYMBOL	RATING	UNIT
Output Sustaining Voltage		$V_{CE(SUS)}$	50	V
Output Current		I_{OUT}	500	mA
Input Voltage		V_{IN}	-0.5 ~ +30	V
Clamp Diode	Reverse Voltage	V_R	50	V
	Forward Current	I_F	500	mA
GND Terminal Current		I_{GND}	2.5	A
Power Dissipation	AP	P_D	1.47	W
	AF		0.54	W
Operating Temperature		T_{opr}	-20 ~ 85	℃
Storage Temperature		T_{stg}	-65 ~ 150	℃



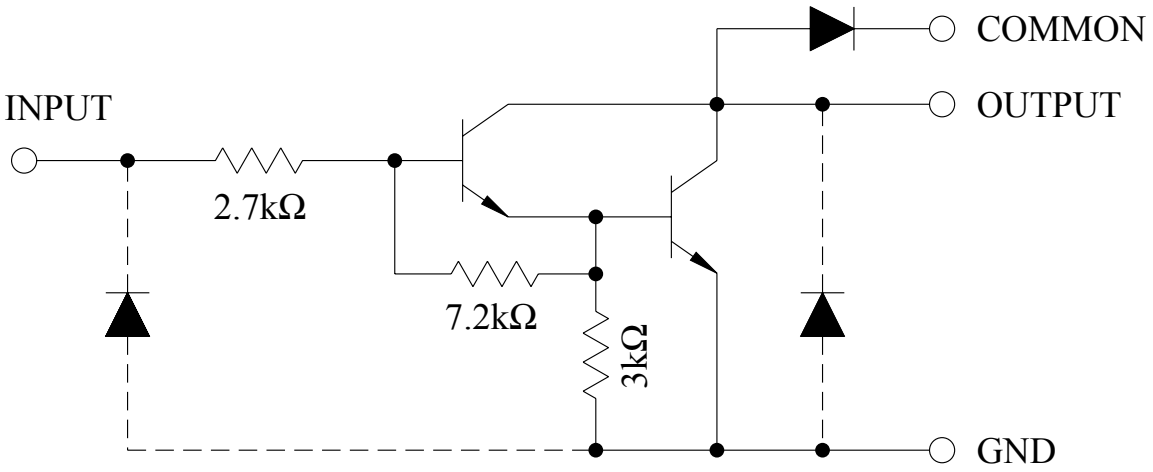
DIM	MILLIMETERS
A	9 88±0 2
B1	3 94±0 2
B2	6 00±0 3
D	0 4±0 1
G	0 15+0 1/-0 05
H	1 63±0 2
L	0 65±0 2
P	1 27
T	0 20+0 1/-0 05

SOP-16

PIN CONNECTION (TOP VIEW)



SCHEMATICS (EACH DRIVER)



RECOMMENDED OPERATING CONDITIONS (Ta=-40 ~ 85℃)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Sustaining Voltage		$V_{CE(SUS)}$		0	-	50	V
Output Current		I_{OUT}	T_{PW}=25ms, DF=10%, 7 Circuits	0	-	400	mA
			T_{PW}=25ms, DF=30%, 7 Circuits	0	-	200	
Input Voltage		V_{IN}		0	-	30	V
Clamp Diode Reverse Voltage		V_R		-	-	50	V
Clamp Diode Forward Current		I_F		-	-	400	mA
Power Dissipation	AP	P_D		-	-	0.52	W
	AF		Ta=Topr(max) *	-	-	0.32	

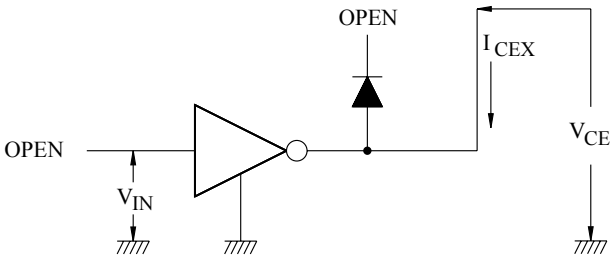
* : on glass epoxy PCB (30 X 30 X 1.6mm Cu50%)

ELECTRICAL CHARACTERISTICS (Ta=25℃, unless otherwise noted)

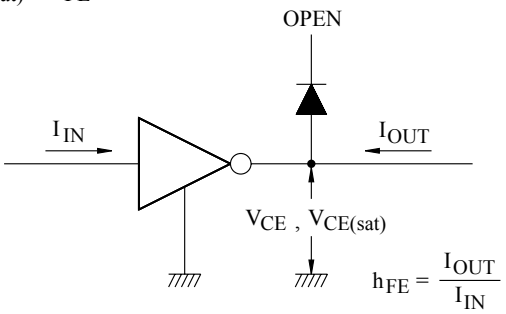
CHARACTERISTICS	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current	I_{CEX}	1	V_{CE}=50V, Ta=25℃	-	-	50	μA
			V_{CE}=50V, Ta=85℃	-	-	100	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	2	I_{OUT}=350mA, I_{IN}=500μA	-	1.2	1.6	V
			I_{OUT}=200mA, I_{IN}=350μA	-	1.0	1.3	
			I_{OUT}=100mA, I_{IN}=250μA	-	0.9	1.1	
Input Current	$I_{IN(ON)}$	3	V_{IN}=3.85V	-	0.93	1.35	mA
	$I_{IN(OFF)}$	4	I_{OUT}=500 A, Ta=70℃	50	65	-	μA
Input Voltage	$V_{IN(ON)}$	5	V_{CE}=2V, I_{OUT}=200mA	-	-	2.4	V
			V_{CE}=2V, I_{OUT}=250mA	-	-	2.7	
			V_{CE}=2V, I_{OUT}=300mA	-	-	3.0	
DC Current Transfer Ratio	h_{FE}	2	V_{CE}=2V, I_{OUT}=350mA	1000	-	-	
Clamp Diode Reverse Current	I_R	6	V_R=50V, Ta=25℃	-	-	50	μA
			V_R=50V, Ta=70℃	-	-	100	
Clamp Diode Forward Voltage	V_F	7	I_F=350mA	-	1.7	2.0	V
Input Capacitance	C_{IN}		V_{IN}=0, f=1MHZ	-	15	25	pF
Turn-ON Delay	t_{ON}	8	V_{OUT}=50V, R_L=163Ω C_L=15pF	-	0.25	1	μs
Turn-OFF Delay	t_{OFF}			-	0.25	1	

TEST CIRCUIT

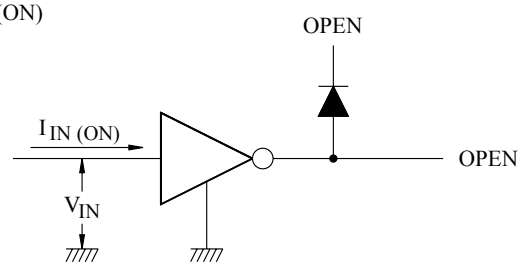
1. I_{CEX}



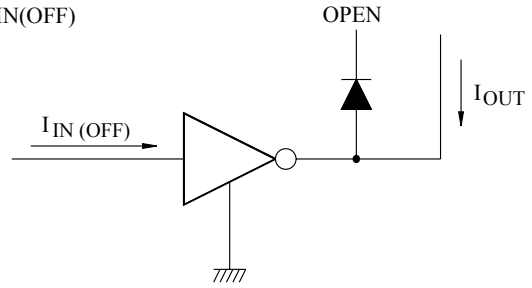
2. $V_{CE(sat)}$, h_{FE}



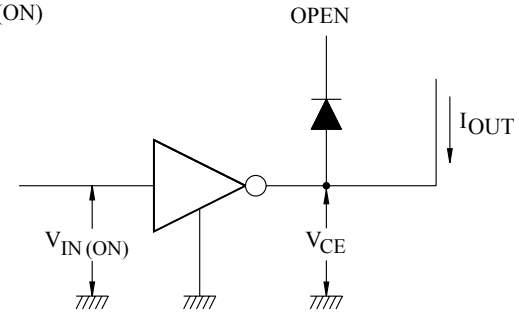
3. $I_{IN(ON)}$



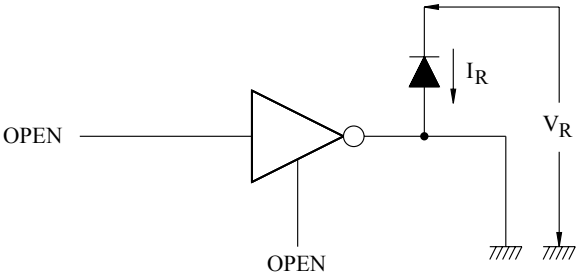
4. $I_{IN(OFF)}$



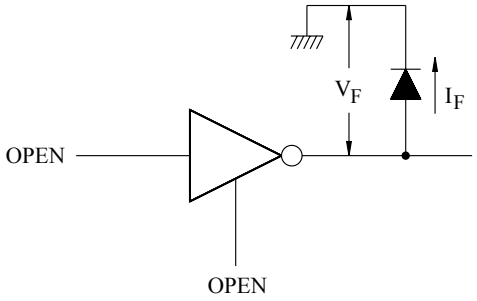
5. $V_{IN(ON)}$



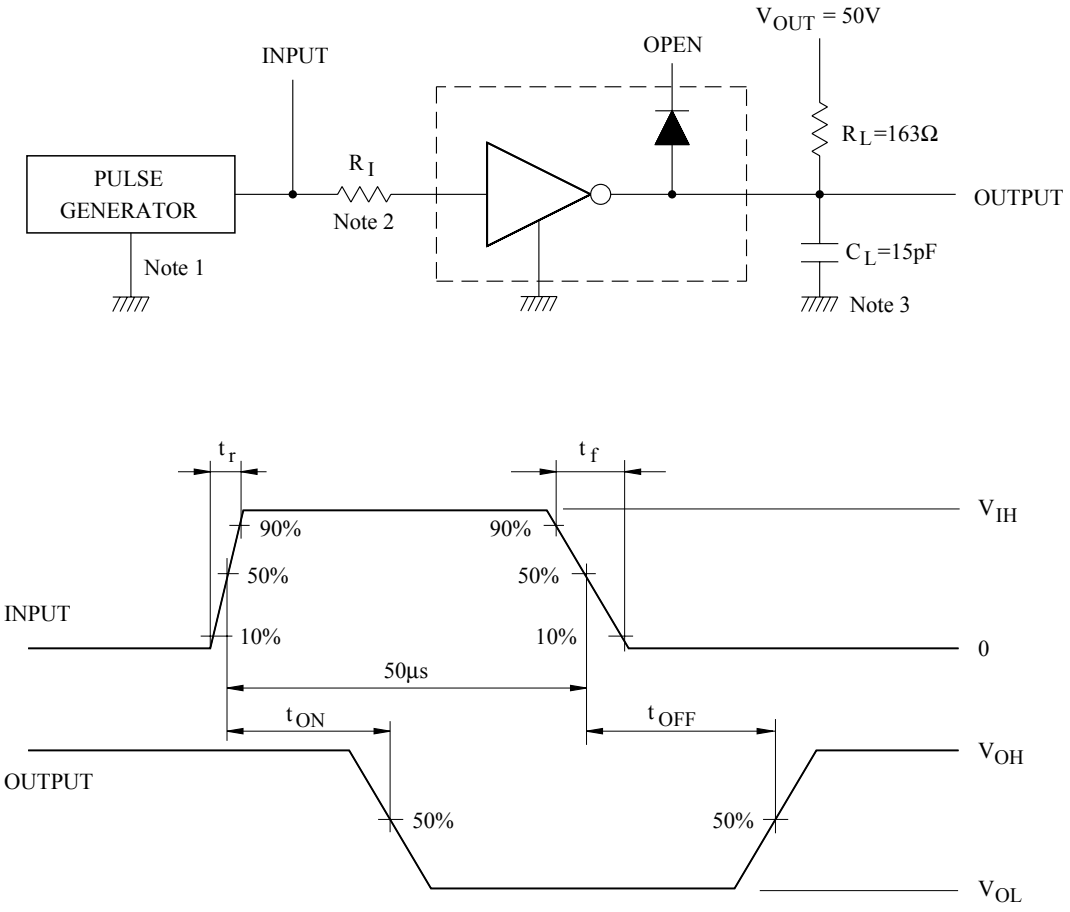
6. I_R



7. V_F



8. t_{ON} , t_{OFF}



Notes : 1. Pulse Width 50μs, Duty Cycle 10%
Output Impedance 50Ω , $t_r \leq$ 5ns, $t_f \leq$ 10ns

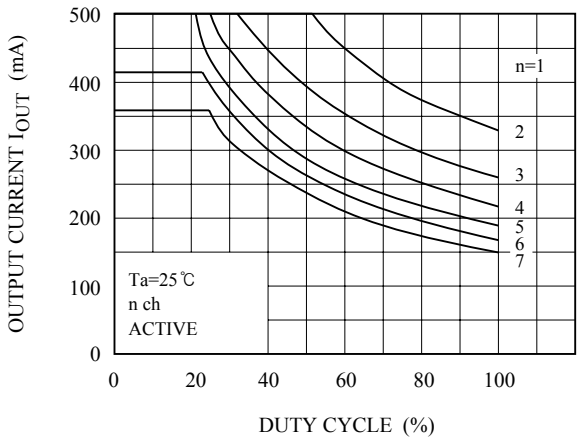
2. See below

Input Conditions

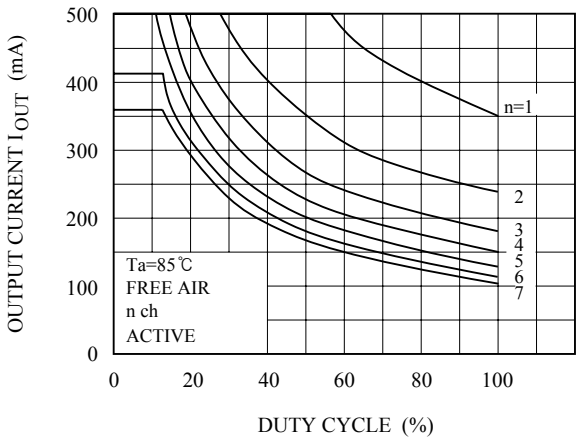
Type Number	R_I	V_{IH}
FD62003AP/AF	0	3V

3. C_L includes probe and Jig capacitance.

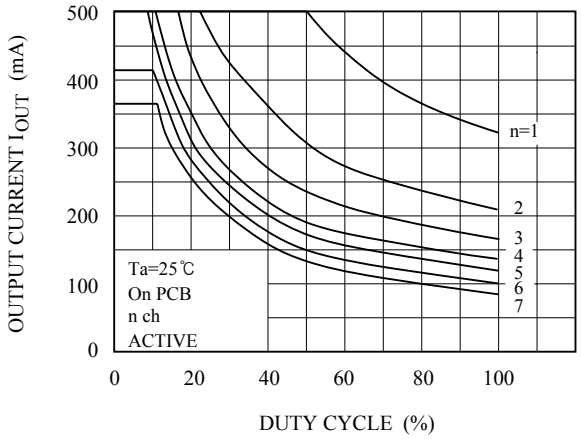
I_{OUT} - DUTY CYCLE



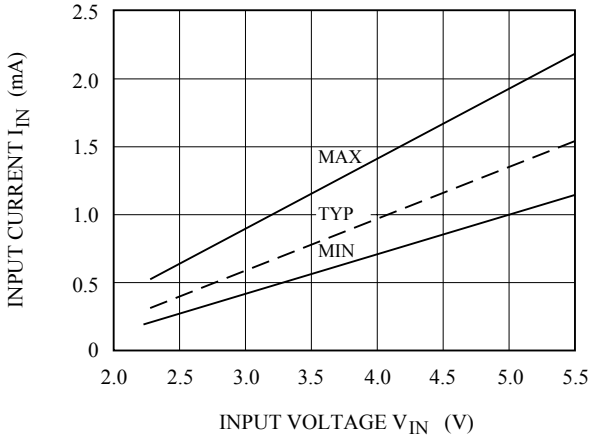
I_{OUT} - DUTY CYCLE



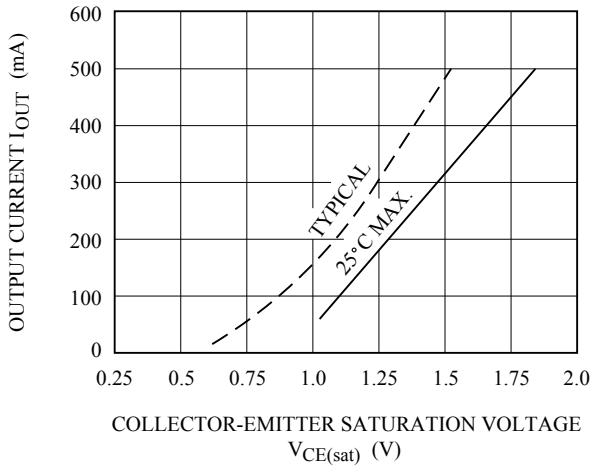
I_{OUT} - DUTY CYCLE



I_{IN} - V_{IN}



I_{OUT} - $V_{CE(sat)}$



P_D - Ta