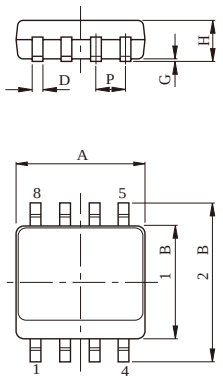
Earth Leakage Detector

Description

The CC54123 is a semiconductor integrated circuit with amplifier for a high speed earth leakage circuit breaker The CC54123 circuit for the amplifying parts of earth leakage circuit breaker consist of differential amplifier, latch circuit and voltage regulator.
It is connected to the secondary node of zero-current transformer (ZCT) which detects leakage current in the both input of the differential amplifier.
Signals amplified by differential amplifier are integrated by an external capacitor, and connects to the input terminal of latch circuit with output suitable for the characteristics of high-speed earth leakage circuit breaker. Latch circuit keeps low in the output till the input voltage reaches the fixed level, and output becomes high when the leakage current is greater than some level. It drives a thyristor connected to the output terminal of latch circuit.



DIM	MILLIMETERS
A	4 85±0 2
B1	3 94±0 2
B2	6 02±0 3
D	0 4±0 1
G	0 15+0 1/-0 05
H	1 63±0 2
L	0 65±0 2
P	1 27
T	0 20+0 1/-0 05

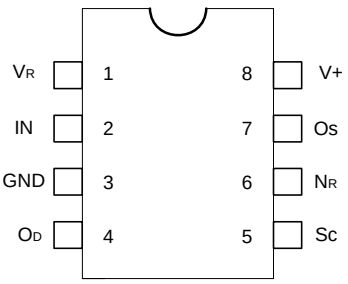
SOP-8

Features

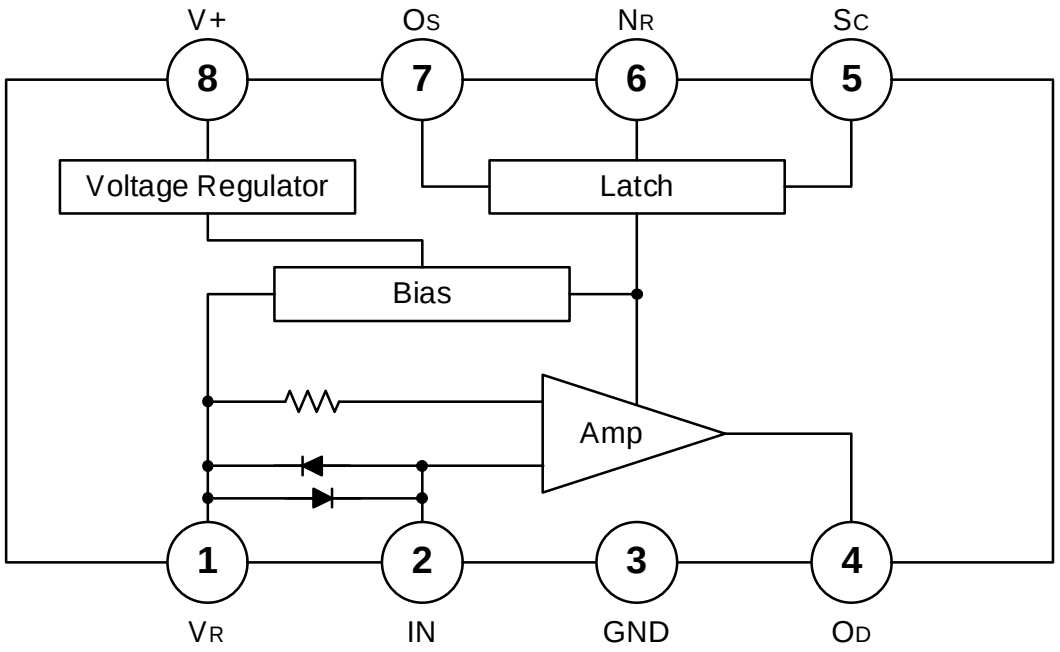
- Good temperature characteristics of input sensitivity current
- High Input Sensitivity (V_T = 13.5mV$_{rms}$ Typ.)
- Low external component count
- High noise and surge-proof
- Low Power consumption (PD = 5mW) 100V/ 200V
- 100V/ 200V Common Built-in Voltage Regulator
- Wide Operating Temperature Range (T_A = -40 to 85℃)

Pin Assignment

(Top view)



Block diagram



Absolute Maximum Rating (T_A = -40 ~ 85°C)

Parameter	Conditions	Symbol	Ratings	Unit
Supply Current		ICC	8	mA
VR pin current	VR ~ IN(Note1)	IVR	250	mA
	VR ~ GND		30	
	IN ~ VR(Note1)		-250	
IN terminal current	IN ~ VR(Note1)	IIN	250	mA
	IN ~ GND		30	
	VR ~ IN(Note1)		-250	
Sc terminal current		ISC	5	mA
Power dissipation		Pd	200	mW
Operating temperature		Topr	-40 ~ 85	°C
Storage Temperature		Tstg	-55 ~ 125	°C

Note1 : Current value between VR and IN, and between IN and VR is less than 1ms in the pulse width, and duty cycle is less than 12%. In applying AC current continuously, it is 100mArms in the off-state.

Remarks : GND terminal(pin③) of the circuit is a basis of all the voltages except differential input clamp voltage of DC electrical characteristics, and direction of current is plus(no signal) in flowing into the circuit and is minus (-signal) in flowing out of it. Maximum value and minimum one are shown as absolute value. Please don't apply voltage whose standard is GND terminal in VR and IN pin.

Recommended Operating Condition (T_A = -40 ~ 85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage when latch circuit is off-state	V+	12			V
Vs - GND Capacitor	Cvs	1			uF
Os - GND Capacitor	Cos			1	uF

Electrical Characteristics (T_A = -40 ~ 85°C, Typical values are at T_A = 25°C)

Parameter	Symbol	Conditions		Temp (°C)	Min	Typ	Max	Unit	Test Circuit
Supply Current1	Is1	V+=12V, VR-VI=30mV		-40	-	-	580	uA	1
				25	-	400	530		
				85	-	-	480		
Trip Voltage	VT	V+=16V. VR-VI=X(Note2)		-40~85	10.0	13.5	17.0	mVrms	2
Differential Amplifier Output Current1	ITD1	V+=16V, VR-VI=30mV VOD=1.2V		25	-12	-	-30	uA	3
Differential Amplifier Output Current2	ITD2	V+=16V, VR-VI=short VOD=0.8V		25	17	-	37	uA	4
Output Current	Io	VSC=1.4V VOS=0.8V	Is1=580 uA	-40	-200	-		uA	5
			Is1=530 uA	25	-100	-			
			Is1=480 uA	85	-75	-			
Sc On Voltage(Note3)	VSC ON	V+=16V		25	0.7	-	1.4	V	6
Sc Input Current	ISC ON	V+=12V		25	-	-	5	uA	7
Output "L" Current	IOSL	V+12V, VOSL = 0.2V		-40~85	200	-	-	uA	8
Input Clamp Voltage	VIC	V+=12V, IIC=20mA		-40~85	4.3	-	6.7	V	9
Differential Input Clamp Voltage	VIDC	IIDC = 100mA		-40~85	0.4	-	2	V	10
Max Current voltage	VSM	ISM=7mA		25	20	-	28	V	11
Supply Current2 (Note4)	Is2	VOS=0.5V, VR-VI=X(Note5)		-40~85	-	-	900	uA	12
Latch Circuit off-state Supply Voltage(Note6)	V+ OFF			25	0.5	-		V	13
Operating time(Note7)	TON	V+=16V, VR-VI=0.3V		25	2	-	4	ms	14

Note2 : When standard value of voltage (50/60Hz) between VR and VI is minimum, and output Os is low-level, or when standard value of voltage (50/60Hz) between VR and VI is maximum, and output Os is high-level, it is considered as a good one.

Note3 : When standard value of voltage VSC ON is minimum, and output Os is low-level, or when standard value of voltage VSC ON is maximum, and output Os is high-level, it is considered as a good one

Note4 : Supply current2 is necessary to keep high in output Os.

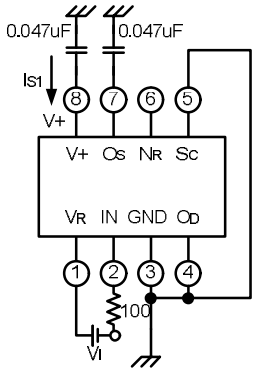
Note5 : After applying 30mV between VR and V1 and shorting between them, it is considered as a good one if standard value of IGT flows out of output Os.

Note6 : After supply voltage applies 12V and output Os is high-level, it is considered as a good one in the standard value of supply voltage and in the low-level of output Os.

Note7 : Operating time is a time from applying fixed input till operating latch circuit in 0.047uF between OD and GND.

Test Circuit

1.



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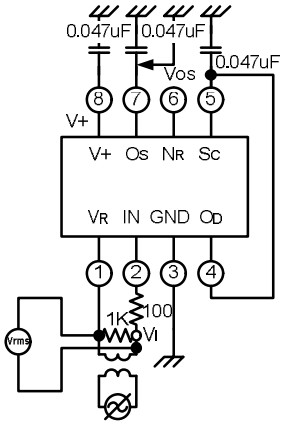

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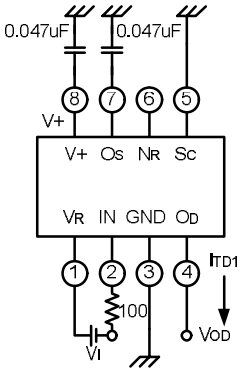

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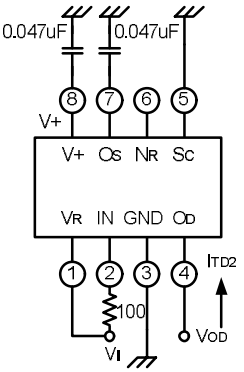

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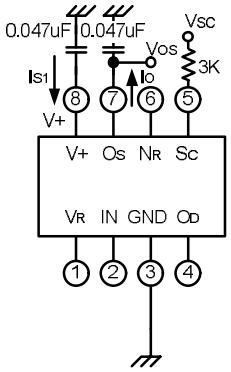

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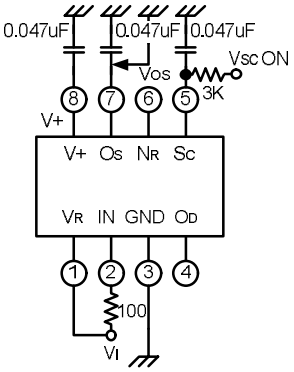

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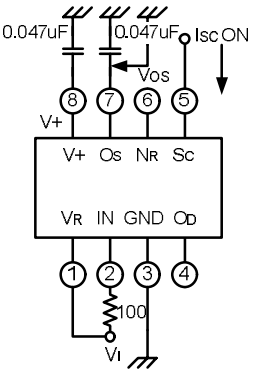

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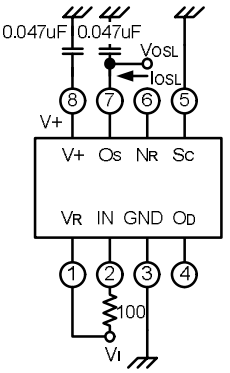

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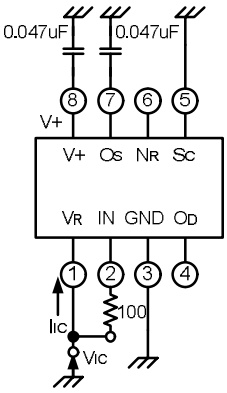

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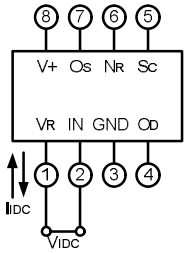

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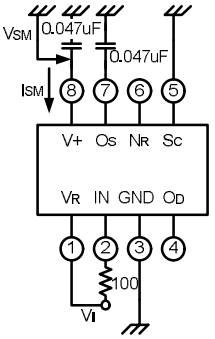

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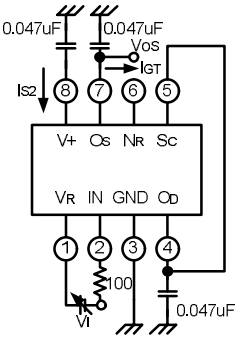

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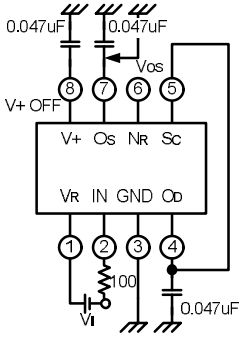

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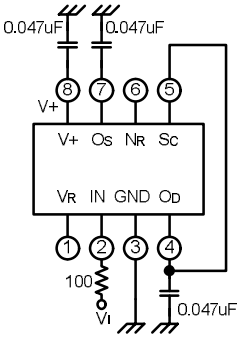
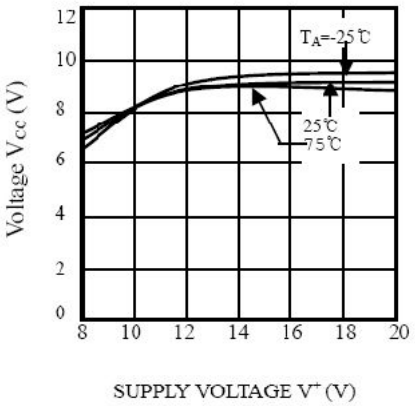


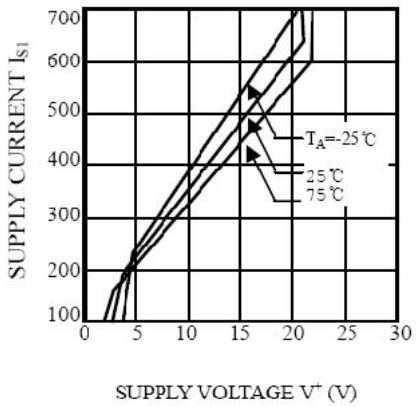
Note : The unit of resistor is ohm. Please insert 0.01uF between pin① and pin③ in test.

Typical Characteristics Curves

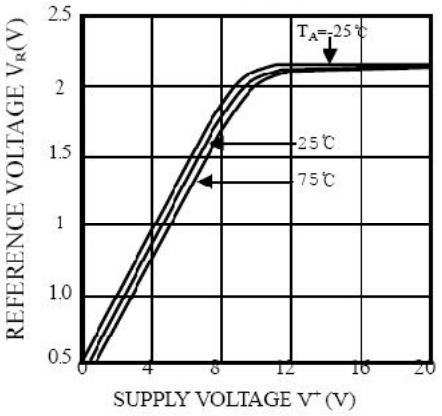
VOLTAE-SUPPLY VOLTAGE



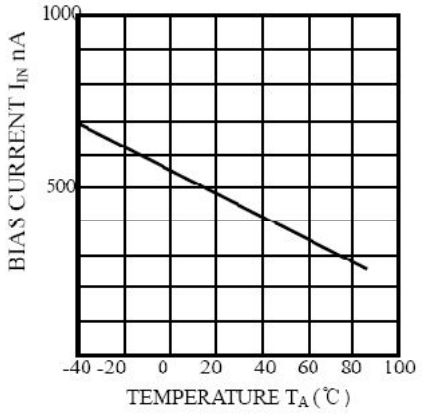
SUPPLY CURRENT-SUPPLY VOLTAGE



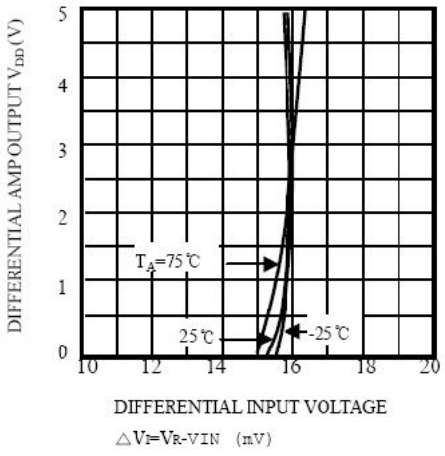
REFERENCE VOLTAGE-SUPPLY VOLTAGE



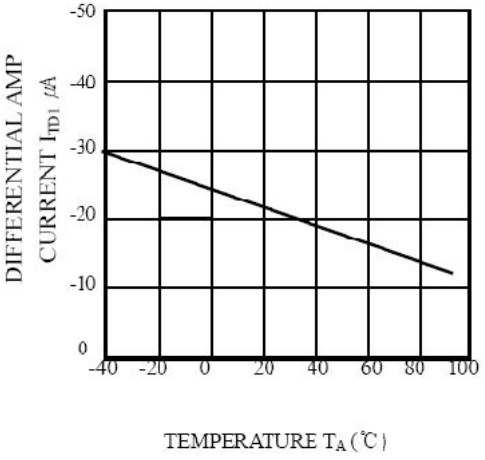
BIAS CURRENT-TEMPERATURE



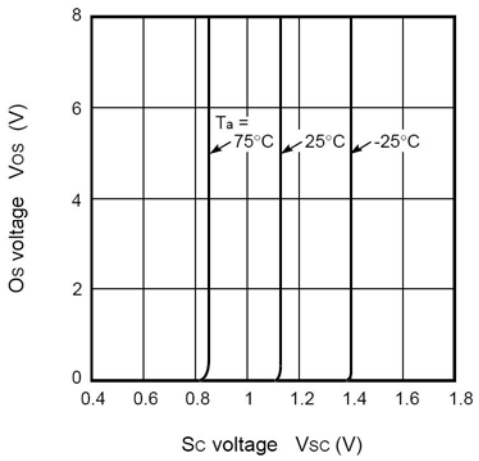
DIFFERENTIAL AMPLIFIER OUTPUT VOLTAGE - DIFFERENTIAL INPUT VOLTAGE



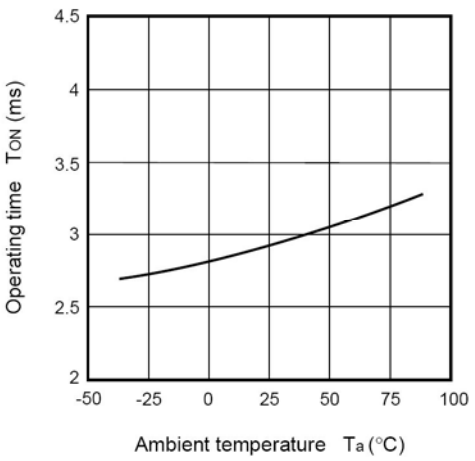
DIFFERENTIAL AMPLIFIER OUTPUT CURRENT-TEMP



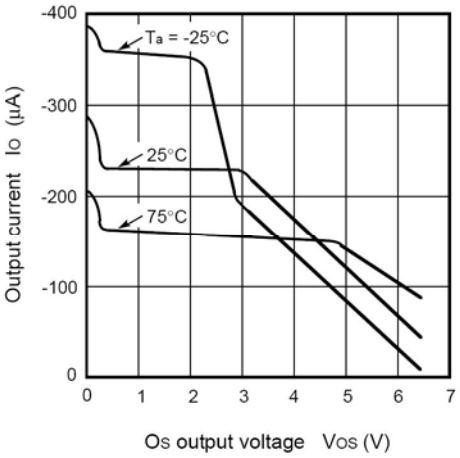
Os voltage vs. Sc voltage



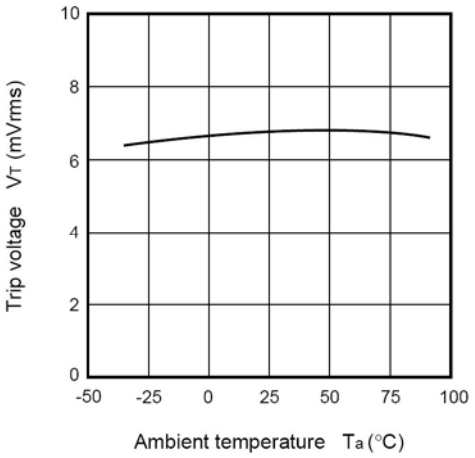
Operating time vs. ambient temperature



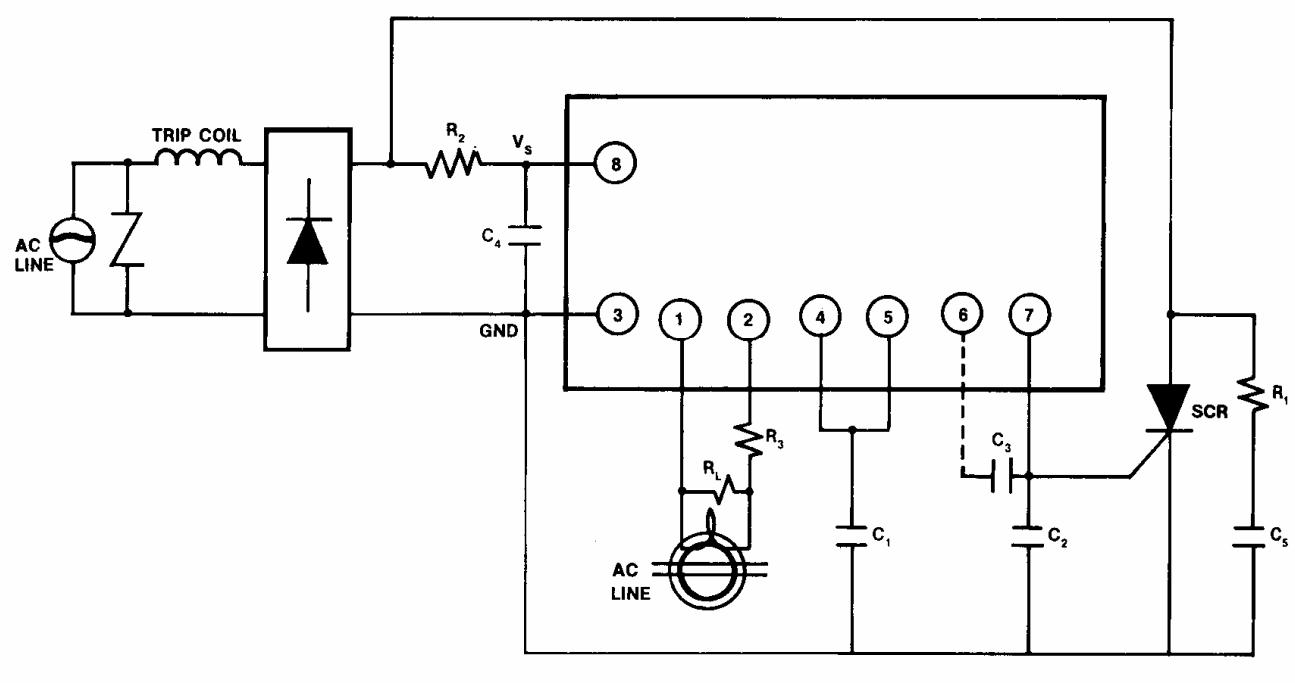
Output current vs. Os output voltage



Trip voltage vs. ambient temperature



Typical Application



Supply voltage circuit is connected as a previous diagram. Please decide constants R1, R2, C4, and C5 of a filter in order to keep at least 12V in V+, when normal supply current flows.

In this case, please connect C4 (more than 1uF) and C2 (less than 1uF). ZCT and load resistance RL of ZCT are connected between input pin① and ②. In this case protective resistance (R3=100Ω) must be inserted. Sensitivity current is regulated by RL, and output of amplifier shows in pin④. External capacitor C1 between pin④ and GND is used for noise removal.

When large current is grounded in the primary side (AC line) of ZCT, the waveform in the secondary side of ZCT is distorted and some signal doesn't appear in the output of amplifier. So please connect a varistor or a diode (2 pcs) to ZCT in parallel.

Latch circuit is used to inspect the output level of amplifier and to supply gate current on the external SCR. When input pin becomes more than 1.1V (Typ.), latch circuit operates and supply gate current in the gate of SCR connected to the output pin⑦.

Pin⑥ can be used in the open state, but please connect capacitor (about 0.047uF) between pin⑥ and pin⑦.