General Description

The FTD6821 are high-efficiency 1.5MHz synchronous step-down DC-DC regulator ICs capable of delivering up to 1.5A output currents, respectively.
The FTD6821 operates over a wide input voltage range from 3V to 5.5V and integrate main switch and synchronous switch with very low RDS(ON) to minimize the conduction loss.

Low output voltage ripple and small external inductor and capacitor sizes are achieved with 1.5MHz switching frequency.

Features

- low Rds(on) for internal switches (top/bottom):
- 3-5.5V input voltage range
- 1.5MHz switching frequency minimizes the external components
- Internal softstart limits the inrush current
- 100% dropout operation
- Compact and thermally enhanced package: SOP8-PP

Applications

- LCD TV WiFi
  Card GPS
- Access Point Router
- Set Top Box

Package Types

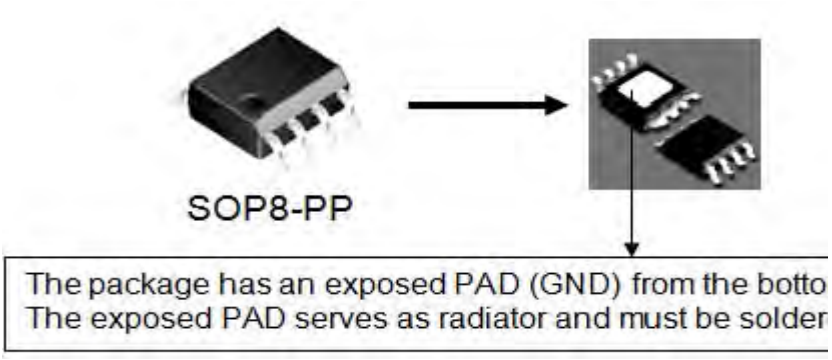


Figure 1. Package Types of FTD6821

Pin Configurations

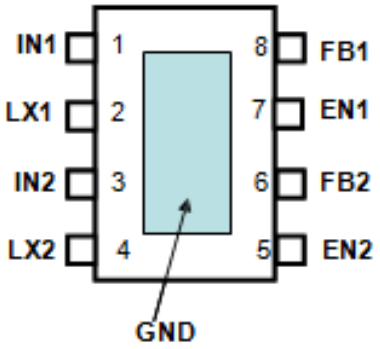
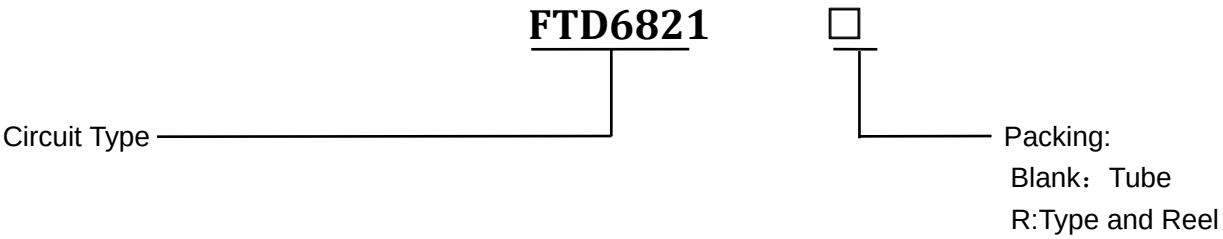


Figure 2 Pin Configuration of FTD6821 (Top View)

Pin Description

Pin Number	Pin Name	Description
7,5	EN1,2	Enable Pin. EN is a digital input that turns the regulator on or off .Drive EN pin high to turn on the regulator, drive it low to turn it off.
Exposed paddle	GND	Ground Pin..
2,4	LX1,2	Power Switch Output Pin. SW is the switch node that supplies power to the output.
1,3	IN1,2	Input pin. Decouple this pin to GND paddle with at least 10uF ceramic cap.
8,6	FB1,2	Feedback Pin. Through an external resistor divider network, FB senses the output voltage and regulates it. The feedback threshold voltage is 0.6V.

Ordering Information



Absolute Maximum Ratings

Note1: Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	-0.3 to 6	V
Feedback Pin Voltage	V_{FB}	Vin+0.6	V
Enable Pin Voltage	V_{EN}	Vin+0.6	V
Power Dissipation	P_D	Internally limited	mW
Operating Junction Temperature	T_J	150	ºC
Storage Temperature	T_{STG}	-65 to 150	ºC
Lead Temperature (Soldering, 10 sec)	T_{LEAD}	260	ºC
ESD (HBM)		2000	V
MSL		Level3	
Thermal Resistance-Junction to Ambient	RθJA	50	ºC / W
Thermal Resistance-Junction to Case	RθJC	10	ºC / W

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Input Voltage	V_{IN}	3	5.5	V
Operating Junction Temperature	T_J	-40	125	ºC
Operating Ambient Temperature	T_A	-40	85	ºC

Electrical Characteristics

V_{CC} = 5V Vout=2.5V,L=2 2uH,Cout=10uF,Imax=1A, T_a = 25℃ unless otherwise specified.

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}		3		5.5	V
Shutdown Supply Current	I_{STBY}	V_{EN}=0V			10	uA
Feedback Voltage	V_{FB}		0.588	0.6	0.612	V
Feedback Bias Current	I_{FB}	V_{FB}=Vin	-50			nA
Oscillator Frequency	F_{OSC}			1.5		MHz
NFET RON	RDS(ON)N			200		mΩ
PFET RON	RDS(ON)N			150		mΩ
PFET Current Limit	ILIM		1.8			A
EN rising threshold	VENH		1.5			V
EN falling threshold	VENL				0.4	V
Input UVLO threshold	VUVLO				2.4	V
UVLO hyesteresis	VHYS			0.1		V
Min ON Time				50		ns
Max Duty Cyele			100			%
Thermal Shutdown Temperature	TSD			160		ºC

Type Application Circuit

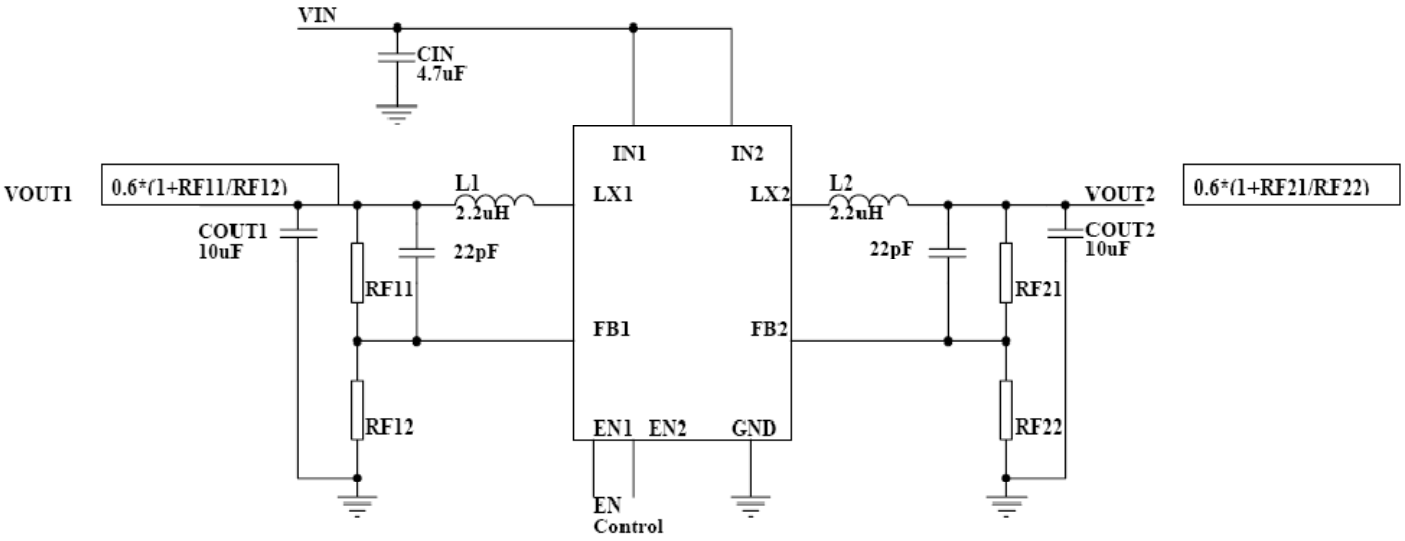
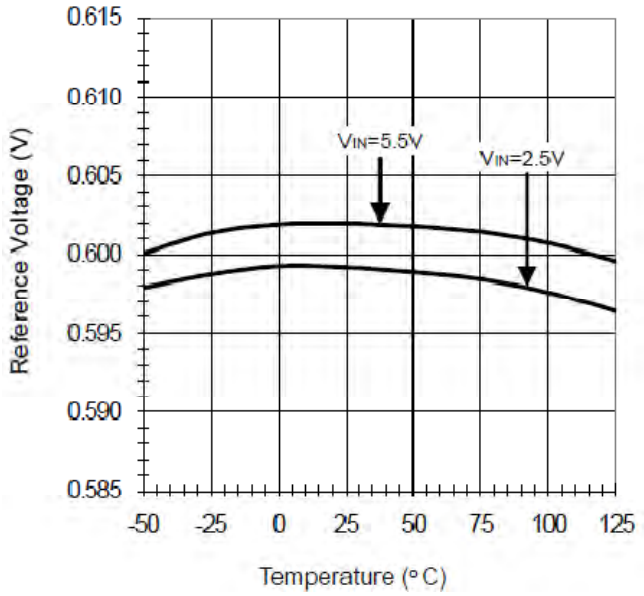


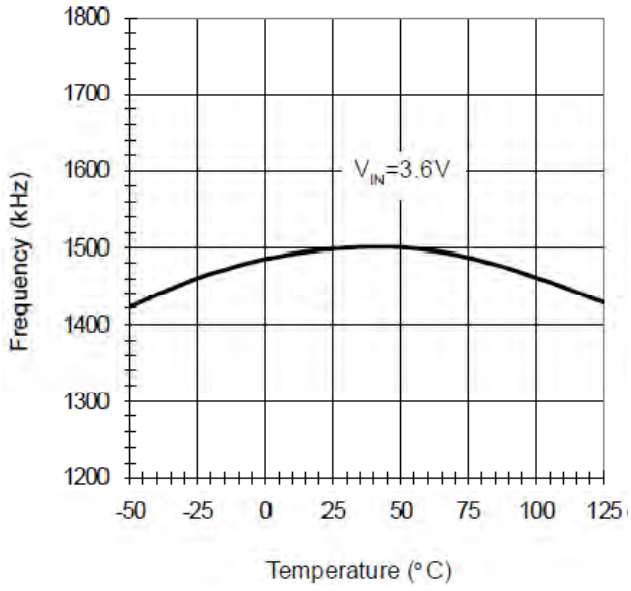
Figure 3. Type Application Circuit of FTD6821

Typical Operating Characteristics

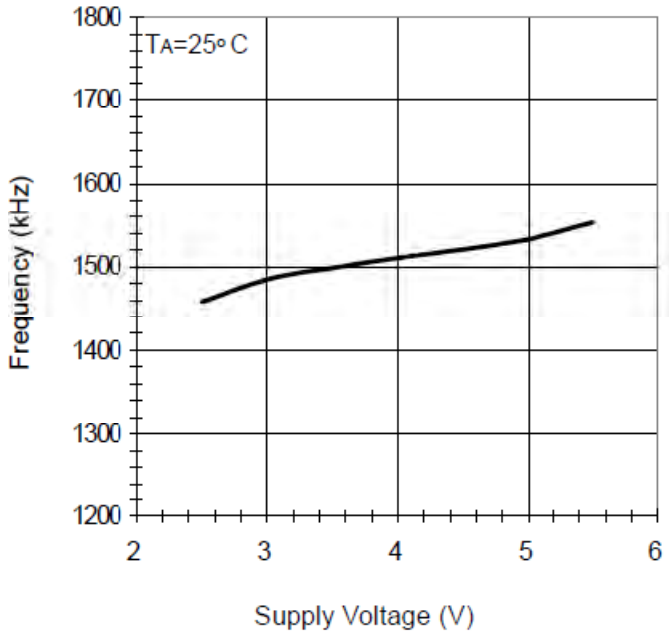
Reference Voltage



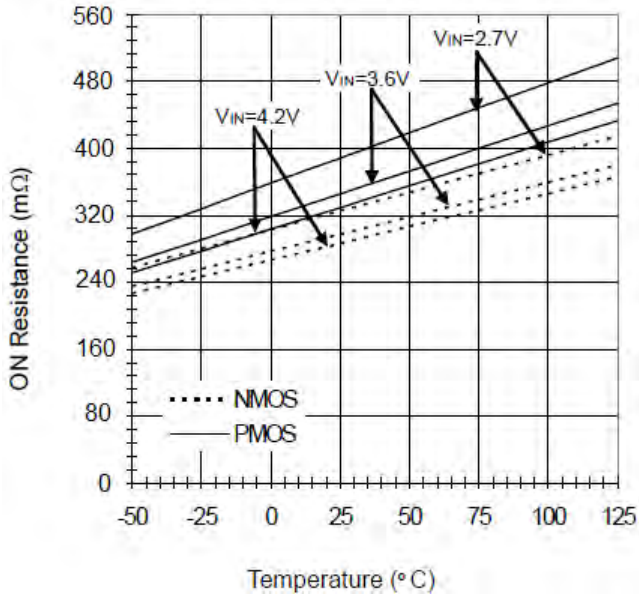
Oscillator Frequency



Oscillator Frequency vs Supply Voltage

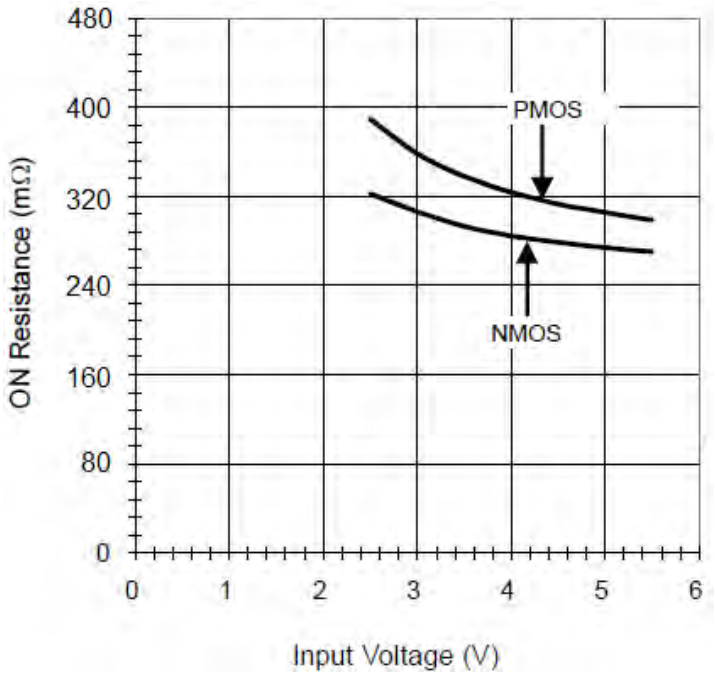


RDS(ON) vs Temperature

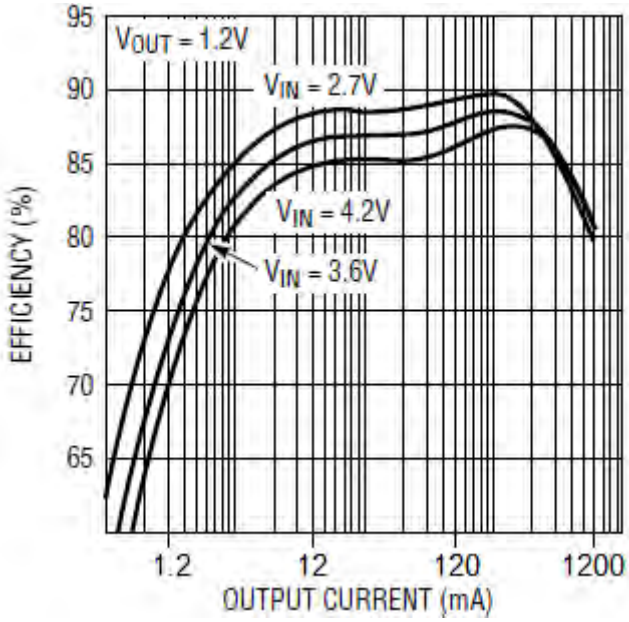


Typical Operating Characteristics(Cont.)

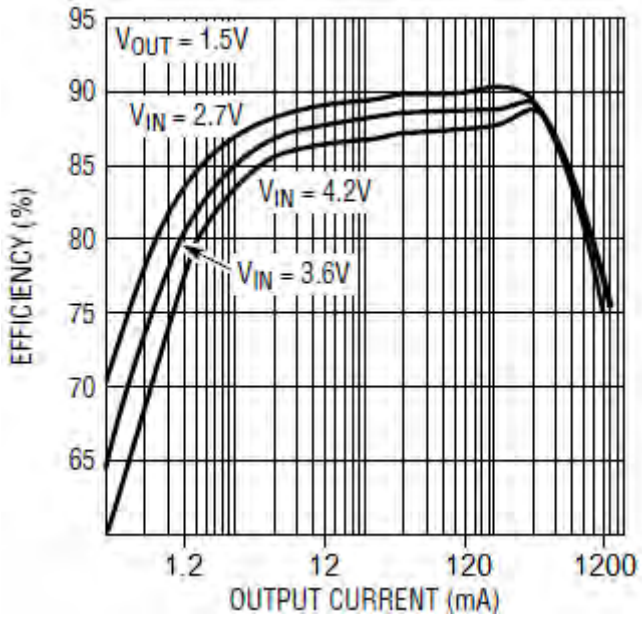
RDS(ON) vs Input Voltage



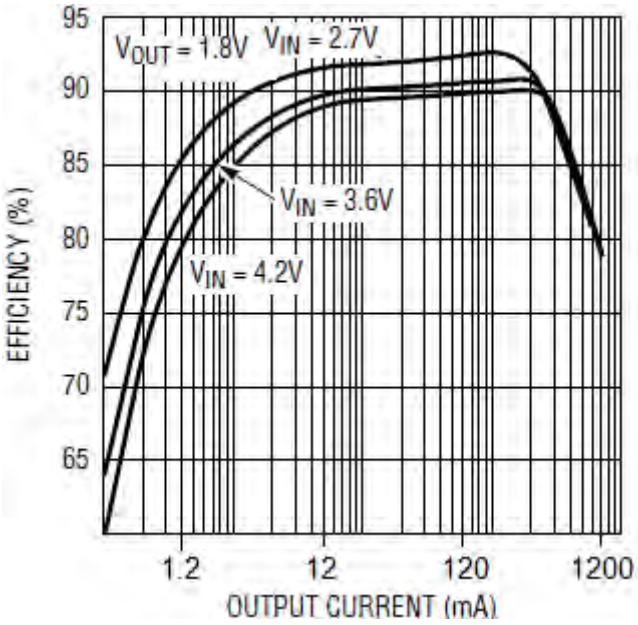
Efficiency vs Output Current



Efficiency vs Output Current

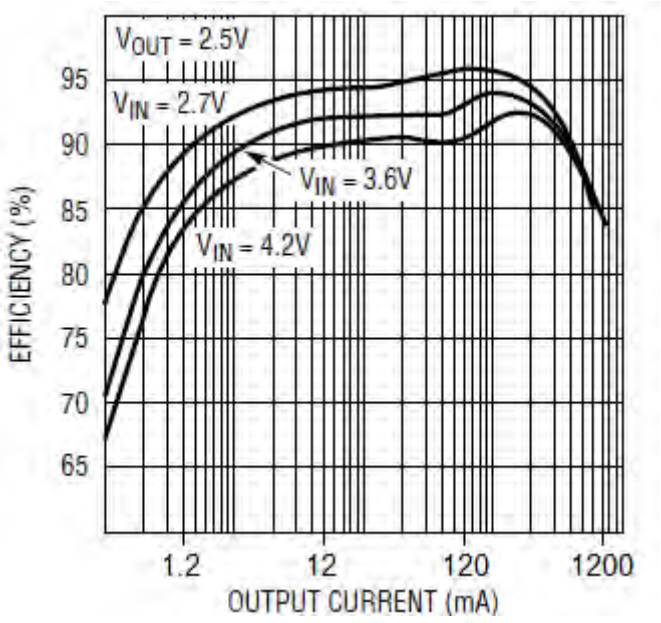


Efficiency vs Output Current

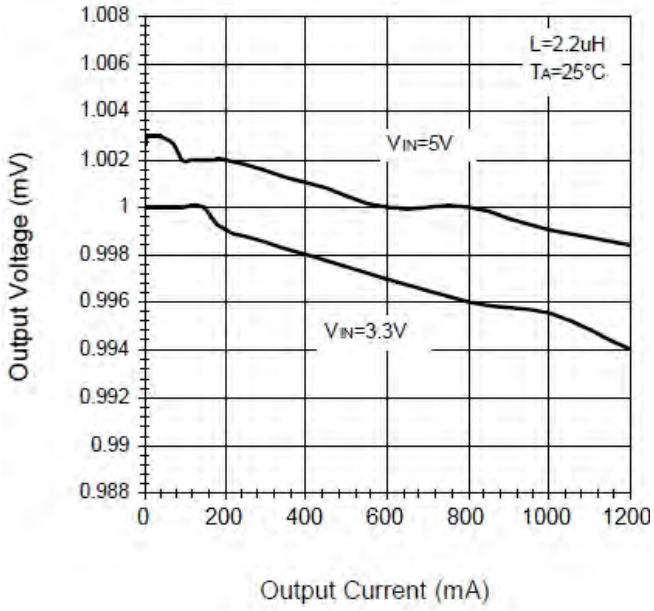


Typical Operating Characteristics(Cont.)

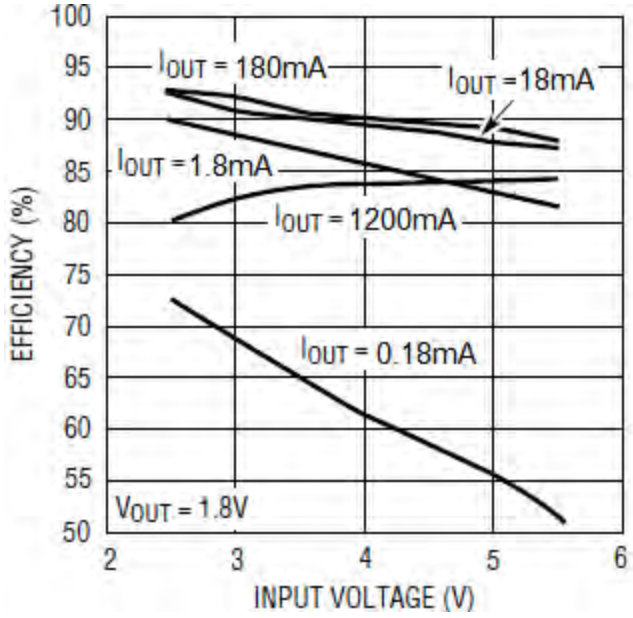
Efficiency vs Output Current



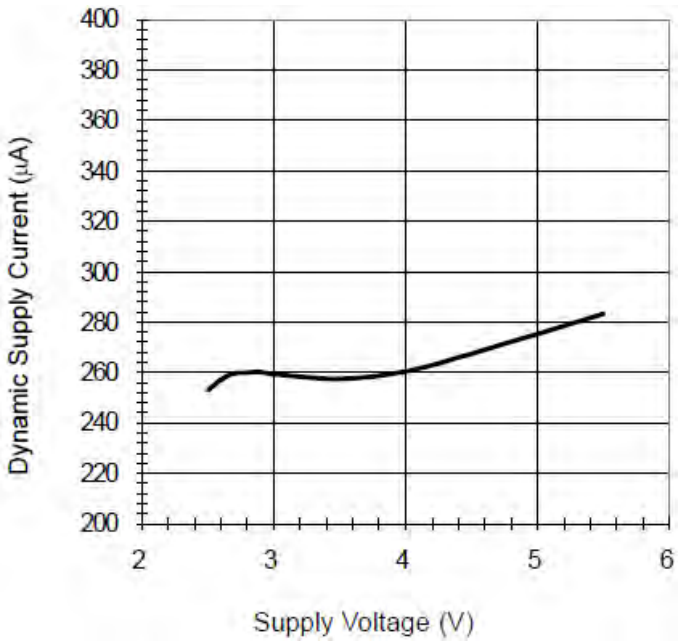
Output Voltage vs Output Current



Efficiency vs Input Voltage

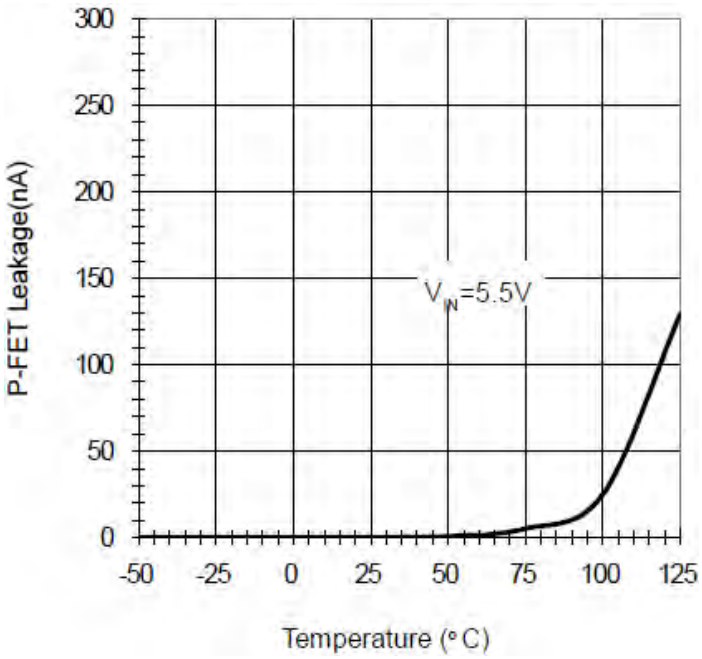


Dynamic Supply Current vs Supply Voltage

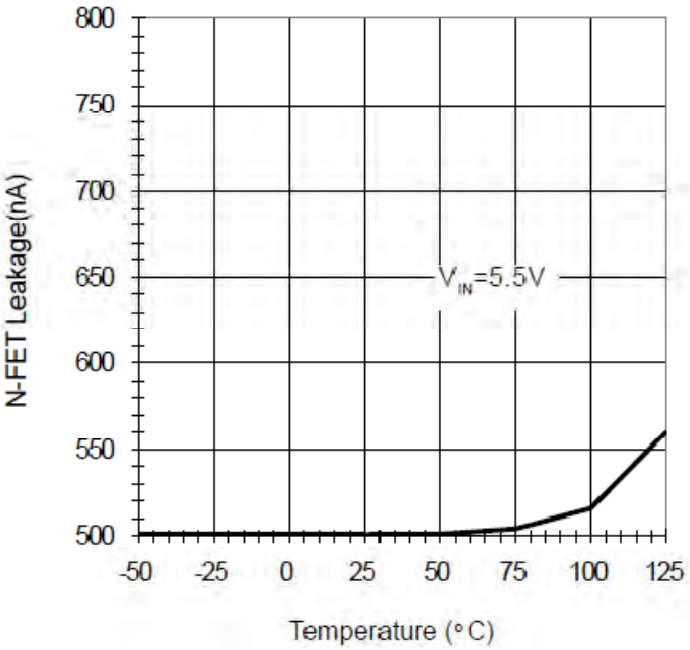


Typical Operating Characteristics(Cont.)

P-FET Leakage vs Temperature



N-FET Leakage vs Temperature



Function Description

Main Control Loop

The FTD6821 uses a constant frequency, current mode step-down architecture. Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. During normal operation, the internal top power MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the current comparator, ICOMP, resets the RS latch. The peak inductor current at which ICOMP resets the RS latch, is controlled by
the output of error amplifier EA. When the load current increases, it causes a slight decrease in the feedback voltage, FB, relative to the 0.6V reference, which in turn, causes the EA amplifier's output voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator IRCMP, or the beginning of the next clock cycle.

Burst Mode Operation

The FTD6821 is capable of Burst Mode operation in which the internal power MOSFETs operate intermittently based on load demand.
In Burst Mode operation, the peak current of the inductor is set to approximately 200mA regardless of the output load. Each burst event can last from a few cycles at light loads to almost continuously cycling with short sleep intervals at moderate loads. In between these burst events, the power MOSFETs and any unneeded circuitry are turned off, reducing the quiescent current to 20mA. In this sleep state, the load current is being supplied solely from the output capacitor. As the output voltage droops, the EA amplifier's output rises above the sleep threshold signaling the BURST comparator to trip and turn the top MOSFET on. This process repeats at a rate that is dependent on the load demand.

Short Circuit Protection

When the output is shorted to ground, the frequency of the oscillator is reduced to about 400kHz, 1/4 the nominal frequency. This frequency foldback ensures that the inductor current has more time to decay, thereby preventing runaway. The oscillator's frequency will progressively increase to 1.5MHz when VFB or VOUT rises above 0V.

Dropout Operation

As the input supply voltage decreases to a value approaching the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor.
An important detail to remember is that at low input supply voltages, the RDS(ON) of the P-channel switch increases (see Typical Performance Characteristics). Therefore, the user should calculate the power dissipation when the FTD6821 is used at 100% duty cycle with low input voltage (See Thermal Considerations in the Applications Information
section).

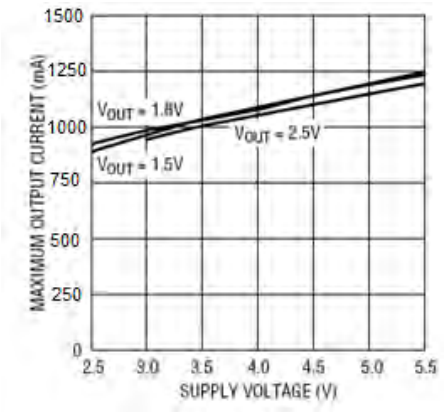
Function Description(Cont.)

Low Supply Operation

The FTD6821 will operate with input supply voltages as low as 2.5V, but the maximum allowable output current is reduced at this low voltage. Figure 2 shows the reduction in the maximum output current as a function of input voltage for various output voltages.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles >40%. However, the FTD6821 uses a patent-pending scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.



Maximum Output Current vs Input Voltag

The basic FTD6821 application circuit is shown in Figure 3. External component selection is driven by the load requirement and begins with the selection of L followed by CIN and COUT.

Inductor Selection

For most applications, the value of the inductor will fall in the range of 1mH to 4.7mH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher VIN or VOUT also increases the ripple current as shown in equation 1. A reasonable starting point for setting ripple current is DIL = 480mA (40% of 1200mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 1320mA rated inductor should be enough for most applications (1200mA + 120mA). For better efficiency, choose a low DC-resistance
inductor.
The inductor value also has an effect on Burst Mode operation. The transition to low current operation begins when the inductor current peaks fall to approximately 200mA. Lower inductor values (higher DIL) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Function Description(Cont.)

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the FTD6821 requires to operate. Table 1 shows some typical surface mount inductors that work well in FTD6821 applications.

PART NUMBER	VALUE (μH)	DCR (Ω MAX)	MAX DC CURRENT (A)	SIZE W × L × H (mm³)
Sumida CDRH3D16	1.5 2.2 3.3 4.7	0.043 0.075 0.110 0.162	1.55 1.20 1.10 0.90	3.8 × 3.8 × 1.8
Sumida CMD4D06	2.2 3.3 4.7	0.116 0.174 0.216	0.950 0.770 0.750	3.5 × 4.3 × 0.8
Panasonic ELT5KT	3.3 4.7	0.17 0.20	1.00 0.95	4.5 × 5.4 × 1.2
Murata LQH32CN	1.0 2.2 4.7	0.060 0.097 0.150	1.00 0.79 0.65	2.5 × 3.2 × 2.0

Table 1. Representative Surface Mount Inductors

CIN and COUT Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle VOUT/VIN. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{required}\ I_{RMS} \cong I_{OMAX}\frac{\left[V_{OUT}(V_{IN}-V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at VIN = 2VOUT, where IRMS = IOUT/2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of COUT is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for COUT has been met, the RMS current rating generally far exceeds the IRIPPLE(P-P) requirement. The output ripple DVOUT is determined by:

$$\Delta V_{OUT} \cong \Delta I_L\left(ESR+\frac{1}{8fC_{OUT}}\right)$$

where f = operating frequency, COUT = output capacitanceand DIL = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since DIL increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Function Description(Cont.)

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the FTD6821's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

However, care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VIN, large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

In the adjustable version, the output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6V\left(1+\frac{R2}{R1}\right)$$

The external resistive divider is connected to the output, allowing remote voltage sensing as Figure4.

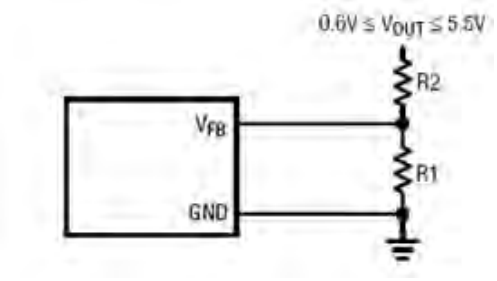


Figure 4:Setting the output Voltage

Vout	R1	R2
1.2V	150K	150K
1.5V	160K	240K
1.8V	150K	300K
2.5V	150K	470K
3.3V	150K	680K

Table 2. Vout VS. R1, R2, Cf Select Table

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses in FTD6821 circuits: VIN quiescent current and I2R losses. The VIN quiescent current loss dominates the efficiency loss at very low load currents whereas the I2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence as illustrated in Figure 5.

Function Description(Cont.)

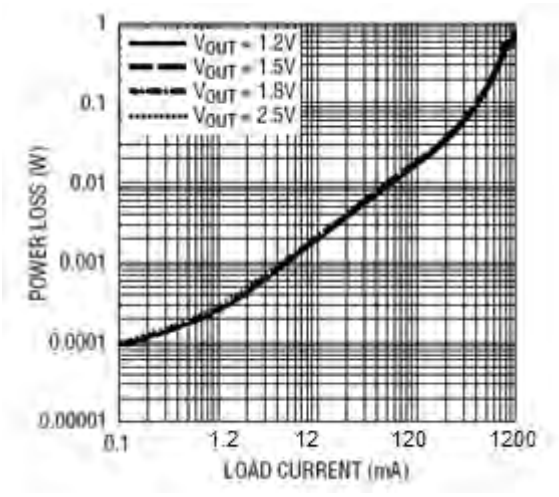


Figure 4:Power Lost VS Load Current

1. The VIN quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, dQ, moves from VIN to ground. The resulting dQ/dt is the current out of VIN that is typically larger than
the DC bias current. In continuous mode, IGATECHG =f(QT + QB) where QT and QB are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thustheir effects will be more pronounced at higher supply voltages.
2. I2R losses are calculated from the resistances of the internal switches, RSW, and external inductor RL. In continuous mode, the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET RDS(ON) and the duty cycle (DC) as follows:

RSW = (RDS(ON)TOP)(DC) + (RDS(ON)BOT)(1 – DC)
The RDS(ON) for both the top and bottom MOSFETs can be obtained from the Typical Performance Charateristics curves. Thus, to obtain I2R losses, simply add RSW to RL and multiply the result by the square of the average output current. Other losses including CIN and COUT ESR dissipative losses and inductor core losses generally account for less than 2% total additional loss.

Thermal Considerations

In most applications the FTD6821 does not dissipate much heat due to its high efficiency. But, in applications where the FTD6821 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.
To avoid the FTD6821 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:
TR = (PD)(qJA)
where PD is the power dissipated by the regulator and qJA is the thermal resistance from the junction of the die to the ambient temperature.
The junction temperature, TJ, is given by:TJ = TA + TR
where TA is the ambient temperature.
As an example, consider the FTD6821 in dropout at an input voltage of 2.7V, a load current of 800mA and an ambient temperature of 70°C. From the typical performance graph of switch resistance, the RDS(ON) of the P-channel switch at 70°C is approximately 0.52W.

Function Description(Cont.)

Therefore,
power dissipated by the part is:
PD = ILOAD 2 • RDS(ON) = 187.2mW
For the SOT-23 package, the qJA is 250°C/ W. Thus, the junction temperature of the regulator is:
TJ = 70°C + (0.1872)(250) = 116.8°C
which is below the maximum junction temperature of 125°C.
Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance (RDS(ON)).

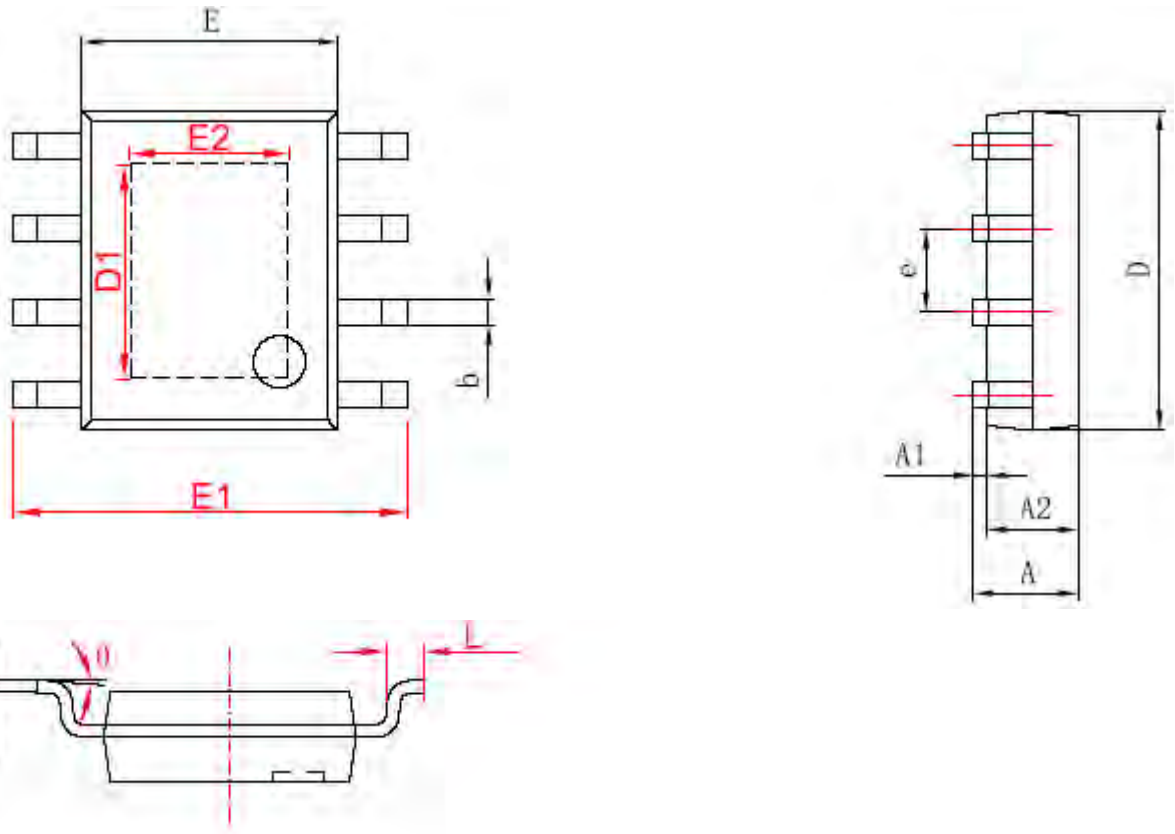
Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current.

When a load step occurs, VOUT immediately shifts by an amount equal to (ΔILOAD • ESR), where ESR is the effective series resistance of COUT. ΔILOAD also begins to charge or discharge COUT, which generates a feedback error signal. The regulator loop then acts to return VOUT to its steadystate value. During this recovery time VOUT can be monitored for overshoot or ringing that would indicate a stability problem. For a detailed explanation of switching control loop theory.
A second, more severe transient is caused by switching in loads with large (>1μF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with COUT, causing a rapid drop in VOUT. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25 • CLOAD).Thus, a 10μF capacitor charging to 3.3V would require a 250μs rise time, limiting the charging current to about 130mA.

Package Information

SOP8 Package Outline Dimensions



	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°