600kHz, 18V, 2.0A Synchronous Step-Down Converter

Features

- High Efficiency: Up to 95%@V_{IN}=12V, V_O=5V
- 600kHz Frequency Operation
- 2.0A Output Current
- No Schottky Diode Required
- 4.5V to 18V Input Voltage Range
- 0.6V Reference
- Excellent Line and Load Transient Response
- Integrated Internal Compensation
- Stable with Low ESR Ceramic Output Capacitors
- Over Current Protection with Hiccup-Mode
- Input Over Voltage Protection (IOVP)
- Thermal Shutdown
- Inrush Current Limit and Soft Start
- Available in DFN2x2-6 Package
- -40°C to +85°C Temperature Range

Description

The FC3470DFN22 is a fully integrated, high efficiency 2.0A synchronous rectified step-down converter.

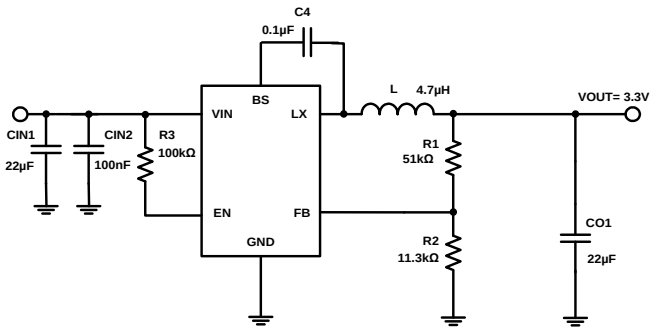
The FC3470DFN22 offers two operation modes, PWM control and PFM Mode switching control, which allows a high efficiency over the wider range of the load.

The FC3470DFN22 requires a minimum number of readily available standard external components and is available in a DFN2x2-6 ROHS compliant package.

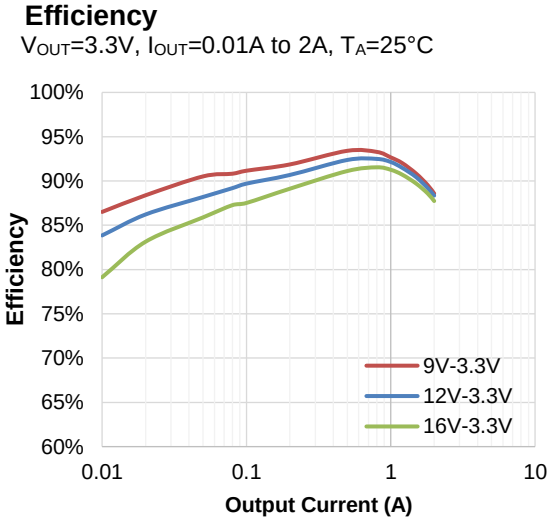
Application

- Distributed Power Systems
- Digital Set Top Boxes
- Flat Panel Television and Monitors
- Notebook computer
- Wireless and DSL Modems

Typical Application



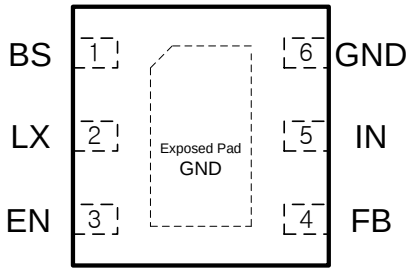
Typical Application Circuits



Absolute Maximum Ratings (Note 1)

Parameter	Min	Max	Unit
Input Supply Voltage, EN	-0.3	20	V
LX Voltages	-0.3	20	V
FB Voltage	-0.3	6	V
BS Voltage	-0.3	23	V
Storage Temperature Range	-65	150	°C
Junction Temperature (Note2)	150		°C
Power Dissipation	1000		mW
Lead Temperature (Soldering, 10s)	260		°C

Package



Top View

Order Information

Part Number	Package	Top Marking	Quantity/Reel
FC3470DFN22	DFN2x2-6	TSDXXX	3000

Pin Function

Pin	Name	Function
1	BS	Bootstrap. A capacitor connected between LX and BS pins is required to form a floating supply across the high-side switch driver.
2	LX	Switching Pin
3	EN	Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and EN should not be floating.
4	FB	Feedback input. Connect FB to the center point of the external resistor divider.
5	IN	Power supply Pin
6	GND	Ground

ESD Rating

Items	Description	Value	Unit
ESD	Human Body Model for all pins	±2000	V

JEDEC specification JS-001

Recommended Operating Conditions

Items	Description	Min	Max	Unit
Voltage Range	IN	4.5	18	V
T_J	Operating Junction Temperature	-40	125	°C

Thermal Resistance (Note3)

Items	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	105	°C/W

Electrical Characteristics

(V_{IN}=12V, V_{OUT}=3.3V, T_A = 25°C, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
Input Voltage Range		4.5		18	V
OVP Threshold			19.3		V
UVLO Threshold		4.0		4.5	V
Supply Current in Operation	V_{EN}=2.0V, V_{FB}=1.1V	0.1	0.3	0.5	mA
Supply Current in Shutdown	V_{EN} =0		5	10	μA
Regulated Feedback Voltage	T_A = 25°C, 4.5V≤ V_{IN} ≤18V	0.588	0.6	0.612	V
High-side Switch On-Resistance			120		mΩ
Low-side Switch On-Resistance			80		mΩ
High-side Switch Leakage Current	V_{EN}=0V, V_{LX}=0V			10	μA
Switch Current Limit	Minimum Duty Cycle	3			A
Oscillation Frequency	V_{FB}=0.6V	500	600	700	kHz
Maximum Duty Cycle			65		%
EN Input High Level Voltage		1.50			V
EN Input Low Level Voltage				0.40	V
Soft Start Time			0.6		ms
Hiccup on Time			1		ms
Hiccup Time Before Restart			4		ms
Minimum On-Time			80		ns
Thermal Shutdown Threshold (Note 4)			155		°C
Thermal Shutdown Hysteresis (Note 4)			25		°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + P_D \times \theta_{JA}$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\,(MAX)} = (T_{J(MAX)}-T_A)/\theta_{JA}$.

Note 3: Measured on JESD51-7, 4-layer PCB.

Note 4: Thermal shutdown threshold and hysteresis are guaranteed by design.

Block Diagram

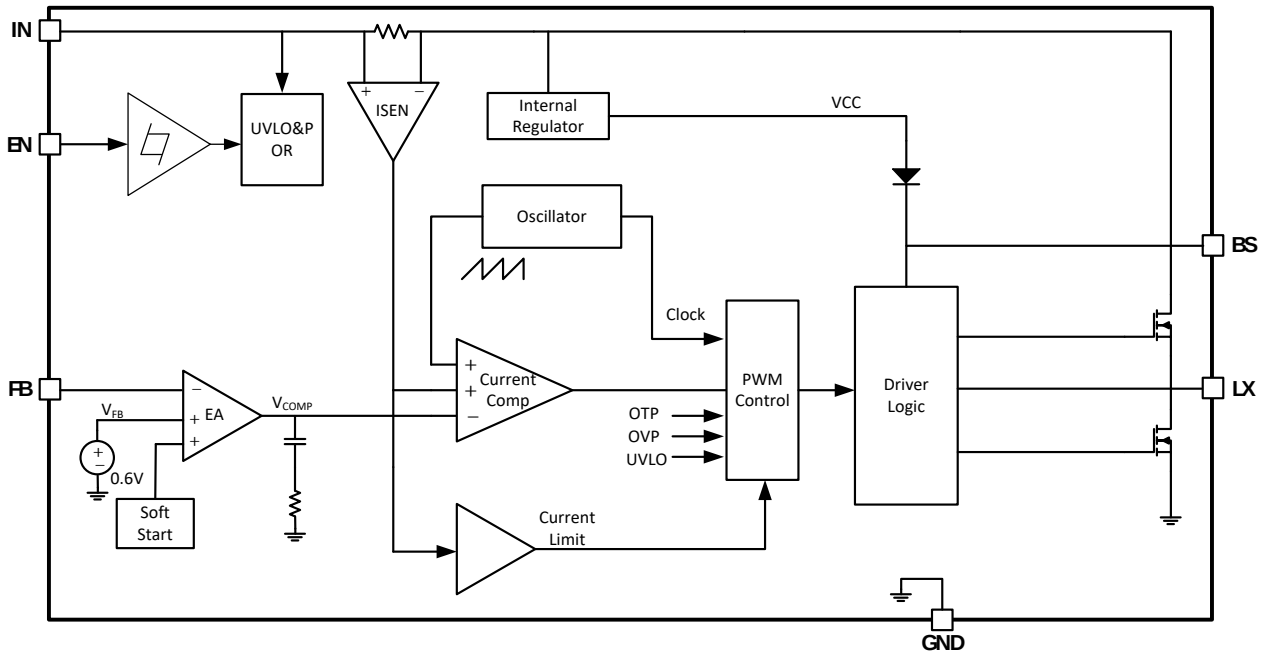
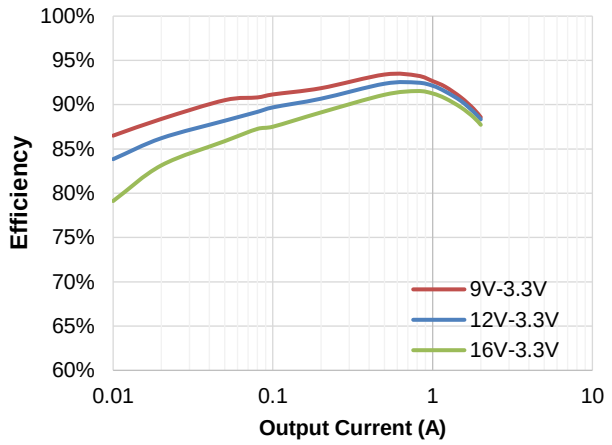


Figure 1. FC3470DFN22 Block Diagram

Typical Performance Characteristics

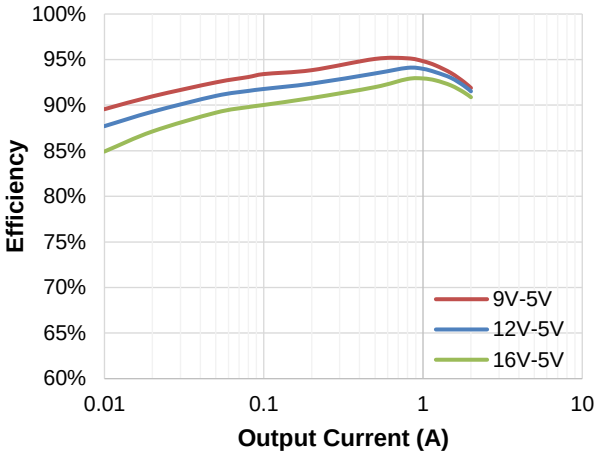
Efficiency

V_{OUT} =3.3V, L=4.7μH, DCR=30mΩ



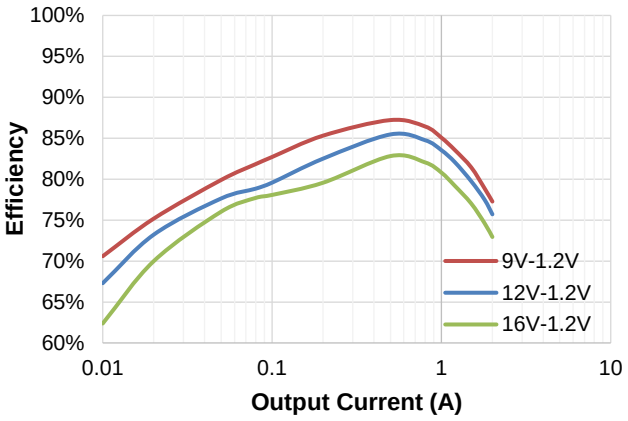
Efficiency

V_{OUT} =5V, L=4.7μH, DCR=30mΩ



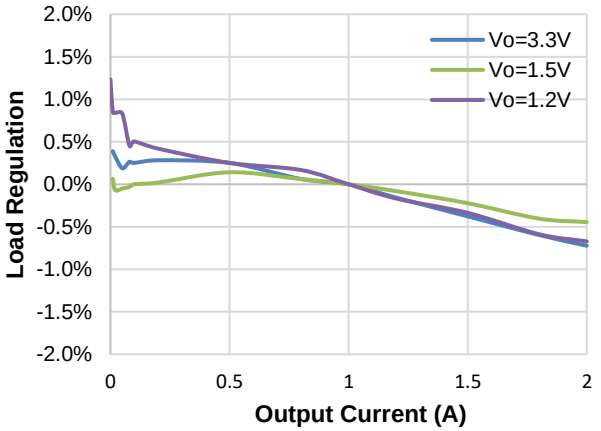
Efficiency

V_{OUT}=1.2V, L=2.2μH, DCR=20mΩ



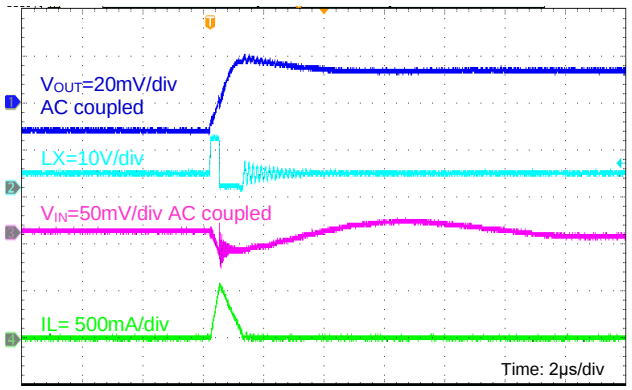
Load Regulation

V_{IN}=12V, T_A=25°C



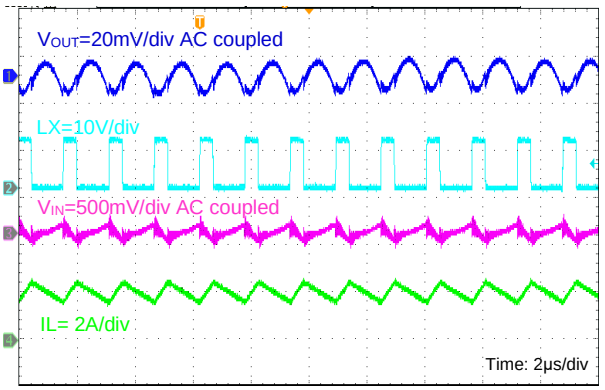
Steady State Operation

V_N = 12V, V_{OUT} = 3.3V, No Load



Steady State Operation

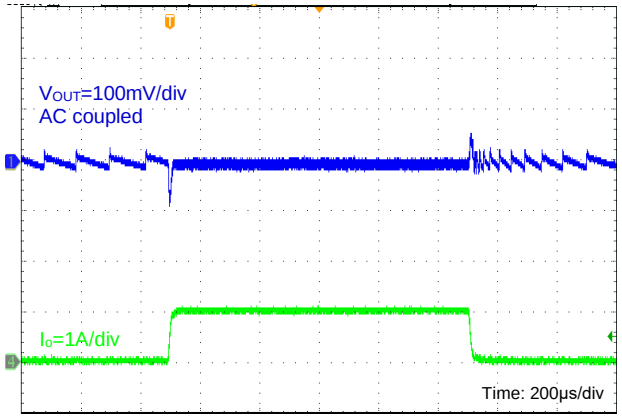
V_{IN} = 12V, V_{OUT} = 3.3V, I_o= 2A



Typical Performance Characteristics(continued)

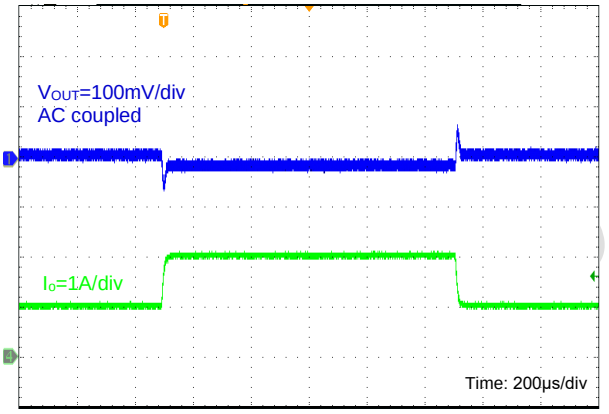
Load Transient

V_{IN} = 12V, V_{OUT} = 3.3V, I_o = 0A to 1A



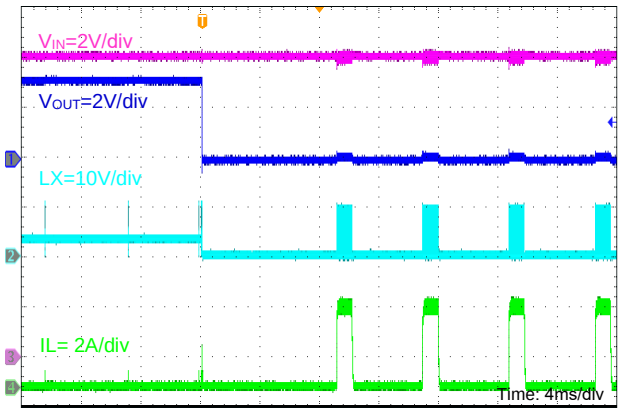
Load Transient

V_{IN} = 12V, V_{OUT} = 3.3V, I_o = 1A to 2A



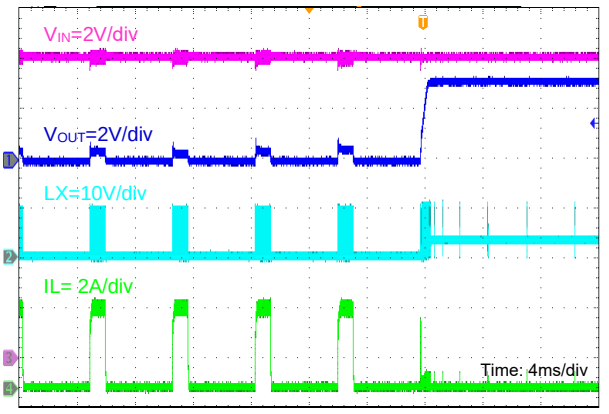
Output Short Entry

V_{IN} =12V, V_{OUT} = 3.3V, No Load



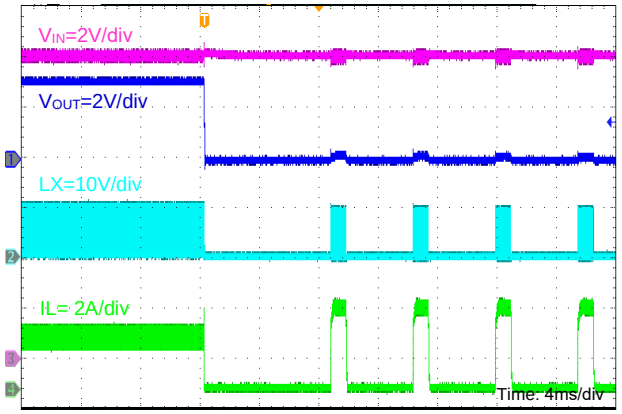
Output Short Recovery

V_{IN}=12V, V_{OUT} = 3.3V, No Load



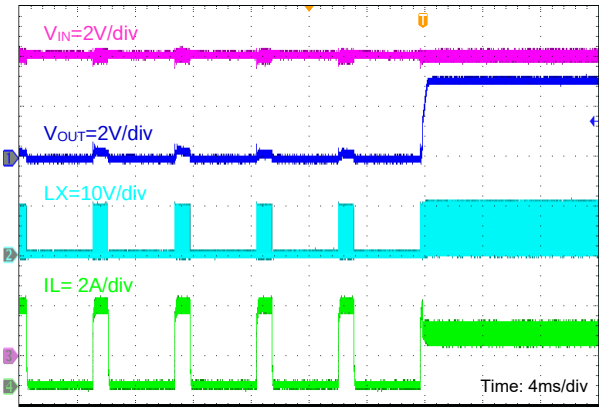
Output Short Entry

V_{IN} =12V, V_{OUT} = 3.3V, I_o = 2A



Output Short Recovery

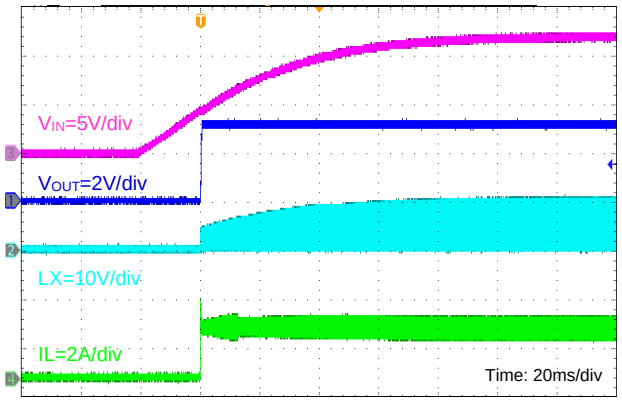
V_{IN}=12V, V_{OUT} = 3.3V, I_o = 2A



Typical Performance Characteristics(continued)

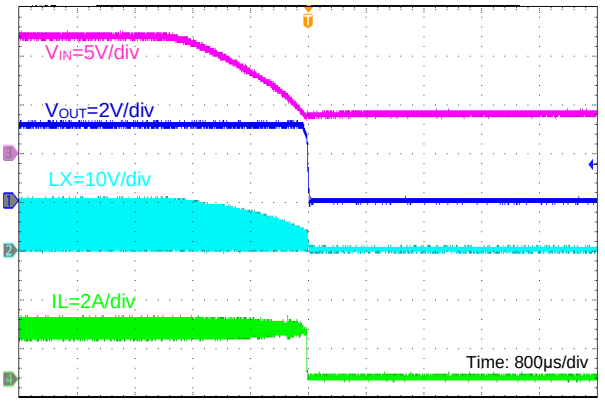
Input Power On

V_{IN} =12V, V_{OUT} = 3.3V, I_o = 2A



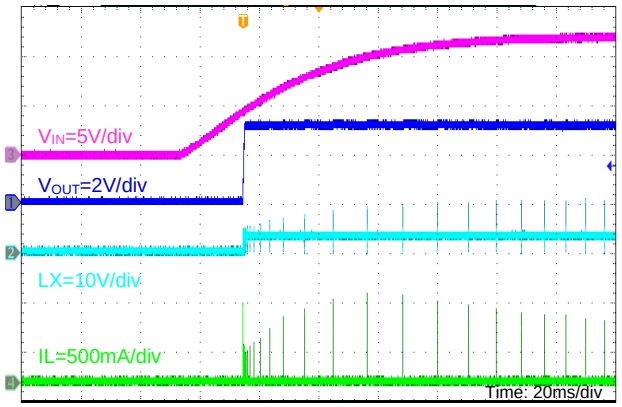
Input Power Down

V_{IN} =12V, V_{OUT} = 3.3V, I_o = 2A



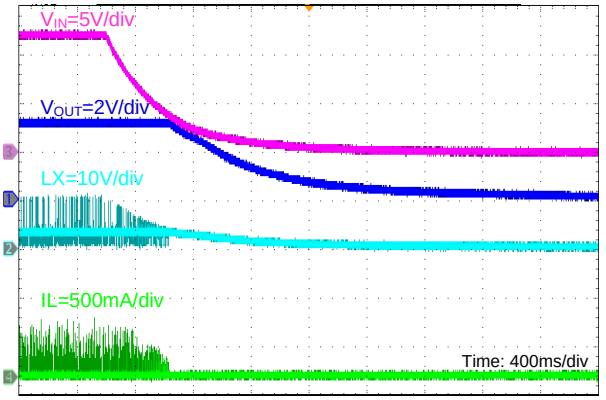
Input Power On

V_{IN} =12V, V_{OUT} = 3.3V, I_o = No Load



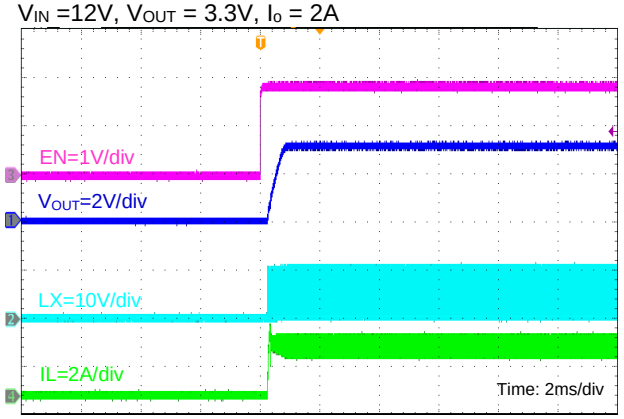
Input Power Down

V_{IN} =12V, V_{OUT} = 3.3V, I_o = No Load



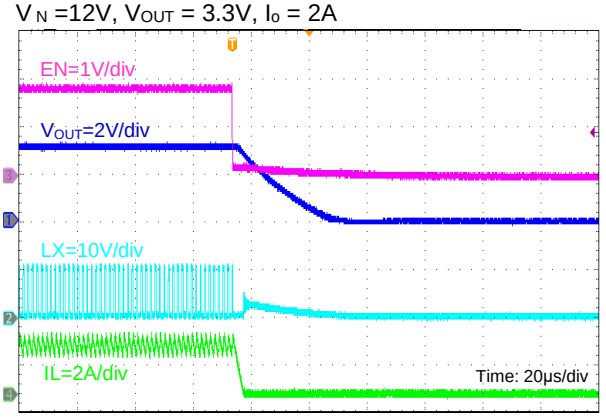
EN Enable

V_{IN} =12V, V_{OUT} = 3.3V, I_o = 2A



EN Disable

V_{IN} =12V, V_{OUT} = 3.3V, I_o = 2A



Operation Description

Internal Regulator

The FC3470DFN22 is a current mode step down DC/DC converter that provides excellent transient response with no external compensation components. This device contains internal, low resistance, high voltage power MOSFET, and operates at a high 600kHz operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal FB reference (V_{FB}=0.6V) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the V_{COMP} voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.6V. When it is lower than the internal reference (V_{FB}), SS overrides V_{FB} so the error amplifier uses SS as the reference. When SS is higher than V_{FB}, V_{FB} regains control. The SS time is internally fixed to 0.6ms.

Over-Current-Protection and Hiccup

The FC3470DFN22 has cycle-by-cycle current limit function. When current limit is triggered, output voltage starts to drop until FB is below the internal under-voltage(UV) threshold, typically 42% below the reference. Once a UV is triggered, the FC3470DFN22 enters hiccup mode to periodically restart the device. This protection mode is especially useful when the output is dead short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The FC3470DFN22 exits the hiccup mode once the over current condition is removed.

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The V_{COMP} voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Application Information

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. Choose R1 to be around 51kΩ for optimal transient response. R2 is then given by:

$$R_2 = \frac{R_1}{V_{out}/V_{FB} - 1}$$

Vout	R1 (kΩ)	R2 (kΩ)
5.1V	51	6.8
3.3V	51	11.3
1.8V	51	25.5
1.55V	51	32.2
1.25V	51	47
1.20V	51	51
1.02V	33	47

Inductor Selection

A 1μH to 4.7μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{out} \times (V_{in} - V_{out})}{V_{in} \times \Delta I_L \times f_{OSC}}$$

Where ΔIL is the inductor ripple current. Choose inductor ripple current to be approximately 30% if the maximum load current, 2A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Output Capacitor Selection

The output capacitor (CO1) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times \left[R_{ESR} + \frac{1}{8 \times f_S \times C_2}\right]$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^{\,2} \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system.
The FC3470DFN22 can be optimized for a wide range of capacitance and ESR values.

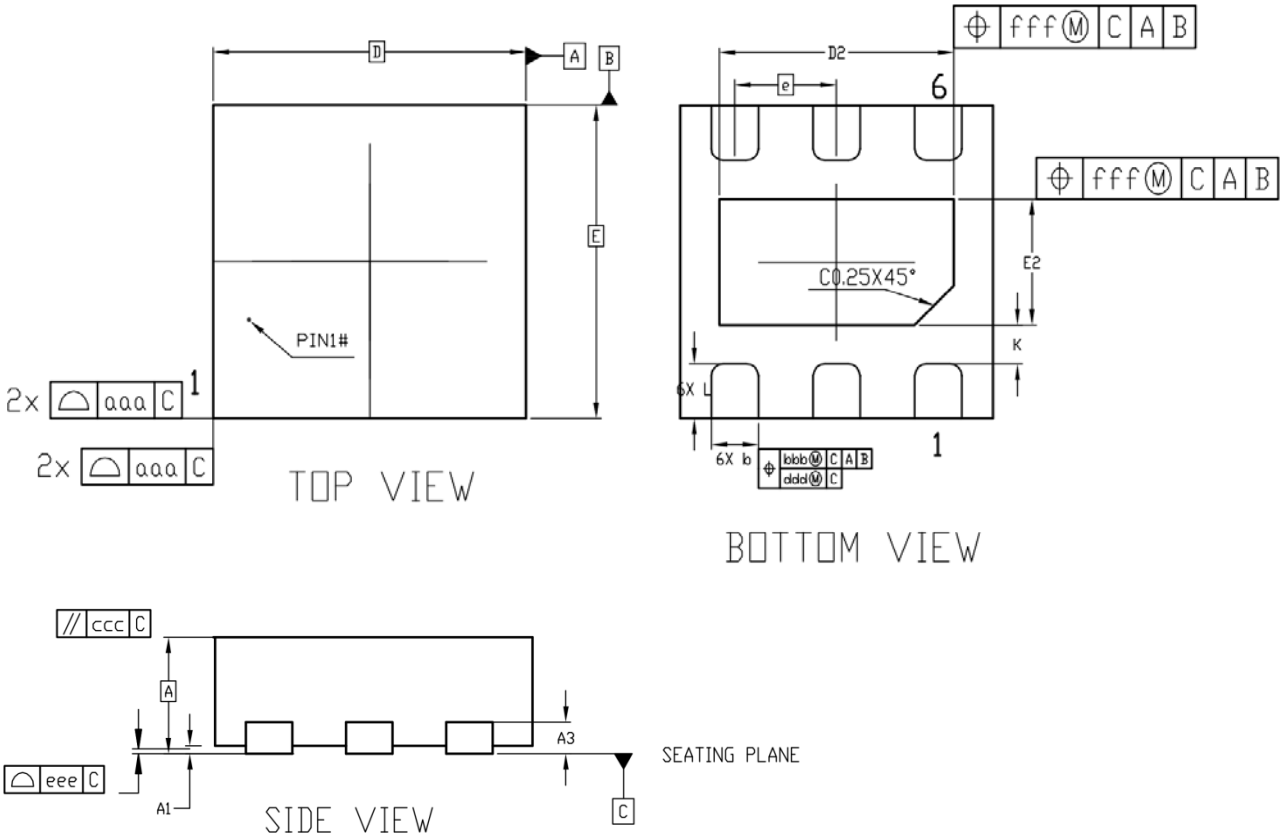
Layout Consideration

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines and take Figure 2 for reference.

1) Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
2) Bypass ceramic capacitors are suggested to be put close to the Vin Pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) VOUT, LX away from sensitive analog areas such as FB.
5) Connect IN, LX, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

PACKAGE INFORMATION

DFN2x2-6



Unit: mm

Symbol	Dimensions In Millimeters			Symbol	Dimensions In Millimeters		
	Min	Nom	Max		Min	Nom	Max
A	0.70	0.75	0.80	e	0.65 BSC		
	0.80	0.85	0.90	L	0.30	0.35	0.40
A1	0	0.02	0.05	K	0.25	-	-
A3	-	0.20 REF	-	aaa	0.15		
b	0.25	0.30	0.35	bbb	0.10		
D	2.00 BSC			ccc	0.10		
E	2.00 BSC			ddd	0.05		
D2	1.40	1.50	1.60	eee	0.08		
E2	0.70	0.80	0.90	fff	0.10		

Note:

1) All dimensions are in millimeters. Angles are in degree.

2) Dimensoning and tolerancing confirm to ASME Y14.5M-1994.

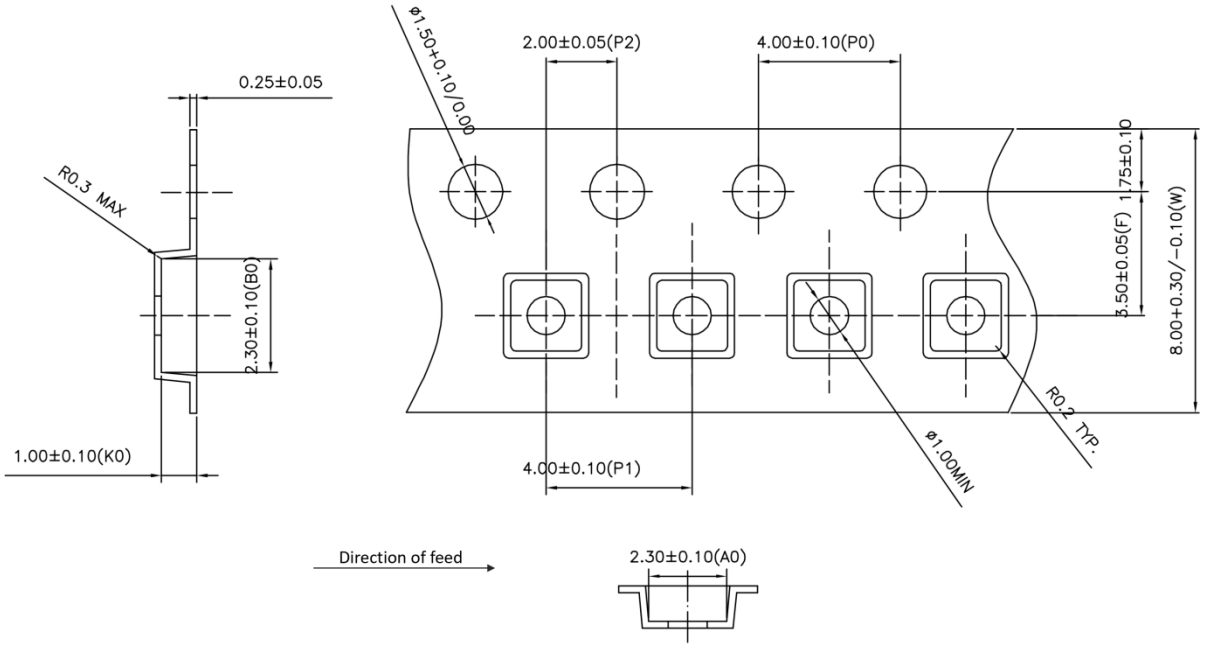
3) Unilateral coplanarity zone applies to the exposed heat sink slug as well as the thermals.

4) Dimension b applies to metallized terminal and is measured between 0.150mm to 0.30mm form the thermal tip. Dimension b should not be measured in radius area.

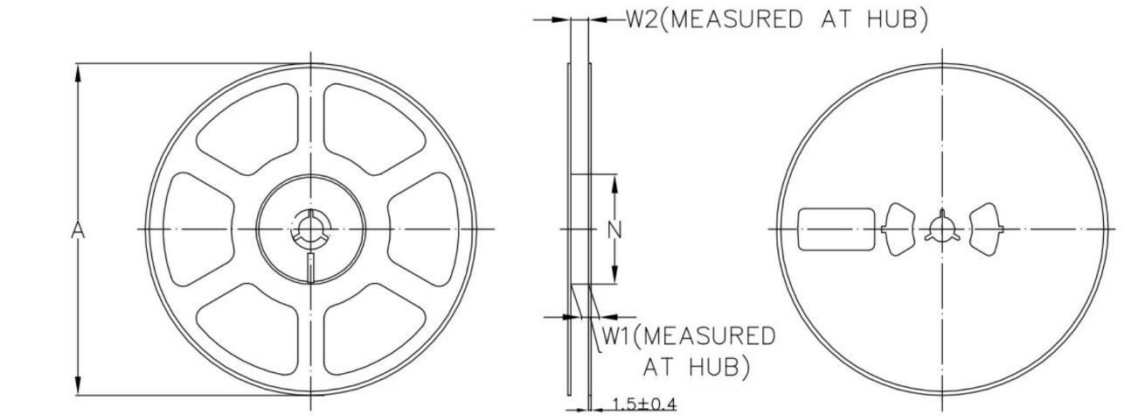
5) All specs take JEDEC MO-229 for reference.

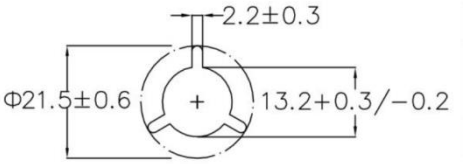
TAPE AND REEL INFORMATION

TAPE DIMENSIONS: DFN2x2-6



REEL DIMENSIONS: DFN2x2-6





Customer Specifications (Unit: mm)				
TAPE WIDTH	A (±1.0)	N (±2.0)	W1 (+1.5/-0)	W2 (Max)
8	178.0	54.0	8.4	14.4

Note:

1) All Dimensions are in Millimeter
2) Quantity of Units per Reel is 3000
3) MSL level is level 3.