2A, 16V, Synchronous Step-Down Converter

General Description

FC6800 develops high efficiency synchronous step-down DC-DC converter capable of delivering 2A load current FC6800 operates over a wide input voltage range from 4.5V to 16V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

FC6800 adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 600kHz under heavy load conditions to minimize the size of inductor and capacitor.

Features

- High Efficiency: Up to 96%
- 600KHz Frequency Operation
- Low $R_{DS(ON)}$ for internal switches (top/bottom):90/70 mΩ
- 4.5-16V input voltage range
- 2A load current capability
- Instant PWM architecture to achieve fast transient responses Internal softstart limits the inrush current
- Thermal Shutdown
- 0.6V reference
- Compact package: SOT-23-6
- Temperature Range:- 40° C to 85° C

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Typical Applications

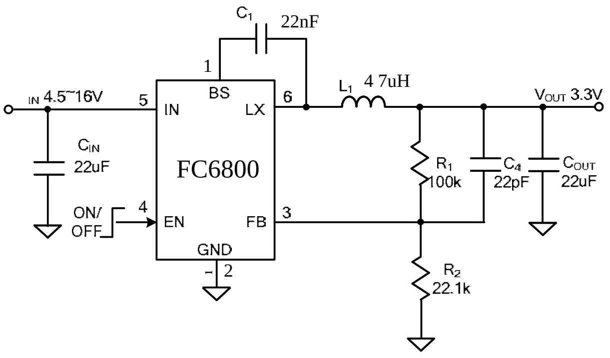
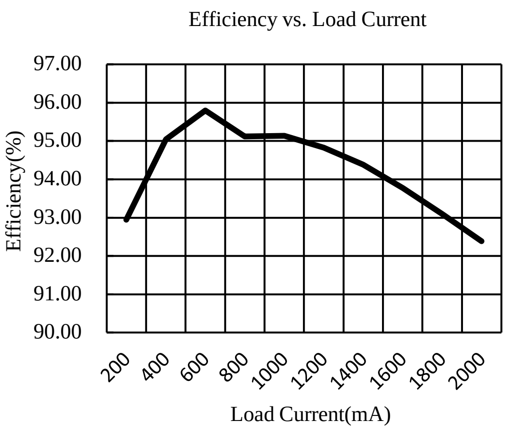


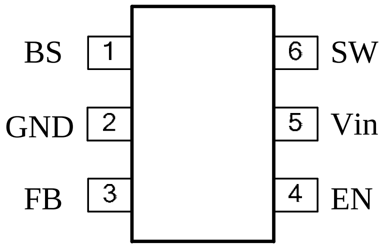
Figure 1. Schematic Diagram



Absolute Maximum Ratings (Note 1)

Input Supply Voltage…………… -0.3V to17V
EN Voltages……………………. -0.3V to 17V
FB Voltages………………………. -0.3V to 6V
SW Voltage……………….-0.3V to (V_{IN}+0. 5V)
BS Voltage…………...(V_{SW}-0.3V) to (V_{SW}+ 5V)
Power Dissipation……………………....0.6W
Thermal Resistance θ_{JC}………......……130° C/W
Thermal Resistance θ_{JA}……………...….170° C/W
Junction Temperature (Note2)……..........150° C
Operating Temperature Range..…- 40° C to 85° C
Lead Temperature(Soldering,10s)............. 300° C
Storage Temperature Range...… - 65° C to 150° C
ESD HBM(Human Body Mode)...................2kV
ESD MM(Machine Mode)………………….200V

Pinout (top view)



(SOT-23-6)

Top Mark: Axyz, (Device code: A, x=year code, y=week code, z= lot number code)

Pin Description

Pin Name	Pin Number	Description
BS	1	Bootstrap. A capacitor connected between SW and BS pins is required to form a floating supply across the high-side switch driver.
GND	2	Analog ground pin.
FB	3	Adjustable version feedback input. Connect FB to the center point of the external resistor divider.
EN	4	Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and enter micro-power shutdown mode.
VIN	5	Power supply Pin
SW	6	Switching Pin

Electaical Characteristics (Note 3)

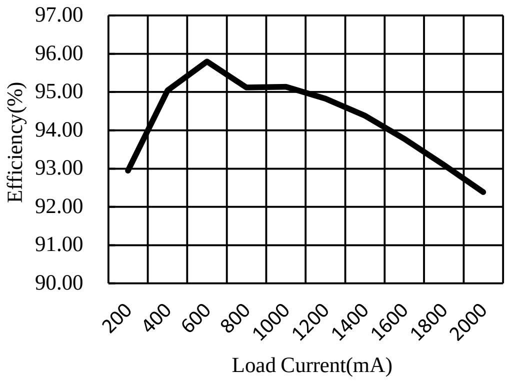
(V_{IN}= 12V,V_{OUT}= 5V, T_A = 25° C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		3.3		16	V
Supply Current in Operation	V_{EN}=2.0V, V_{FB}=1.1V		0.4	0.6	mA
Supply Current in Shutdown	V_{EN} =0 or EN = GND		1		µ A
Regulated Feedback Voltage	T_A = 25° C, 4.5V$\leqslant V_{IN} \leqslant$18V	0.588	0.6	0.612	V
High-Side Switch On-Resistance			90		mΩ
Low-Side Switch On-Resistance			70		mΩ
High-Side Switch Leakage Current	V_{EN}=0V, V_{SW}=0V		0	10	µ A
Upper Switch Current Limit	Minimum Duty Cycle		3		A
Oscillation Frequency			0.6		MHz
Maximum Duty Cycle	V_{FB}=0.6V		92		%
Minimum On-Time			60		nS
Thermal Shutdown			160		℃

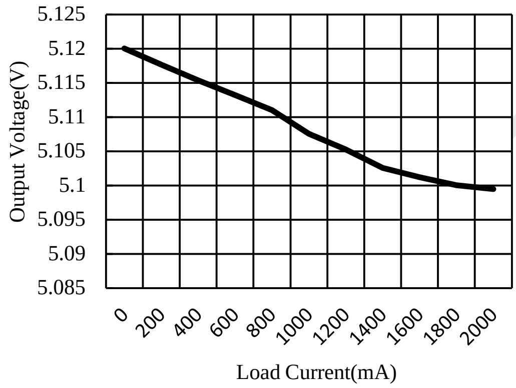
Note1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
Note2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:$T_J = T_A + (P_D)$ x (170° C/W).
Note3: 100% production test at +25° C. Specifications over the temperature range are guaranteed by design and characterization.

Typical Performance characterstice

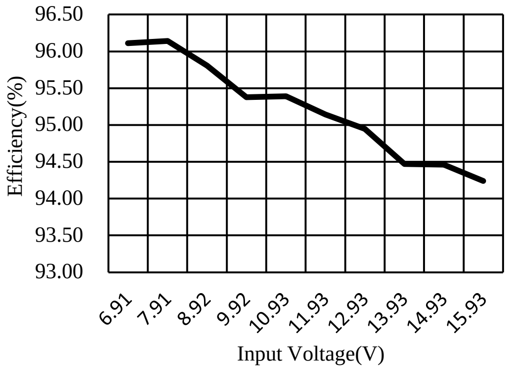
Efficiency vs. Load Current



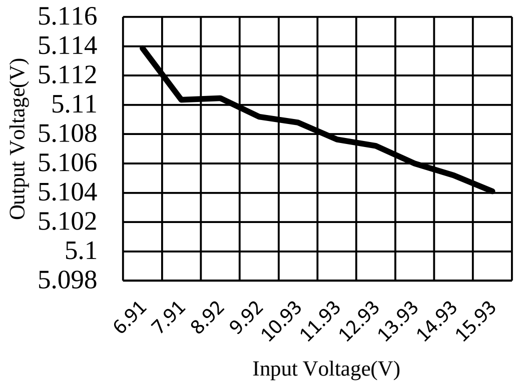
Load Regulation



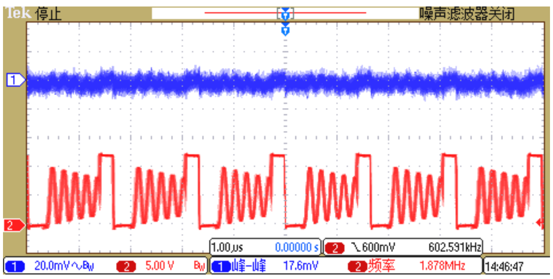
Efficiency vs. Input Voltage



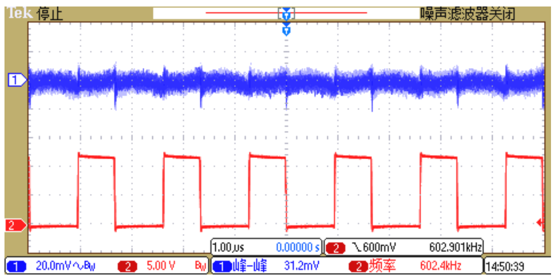
Line Regulation



PFM MODE (CH1:$V_{OUT(ripple)}$ CH2:V_{SW})



PWM MODE(CH1:$V_{OUT(ripple)}$ CH2:V_{SW})



Functional Block Diagram

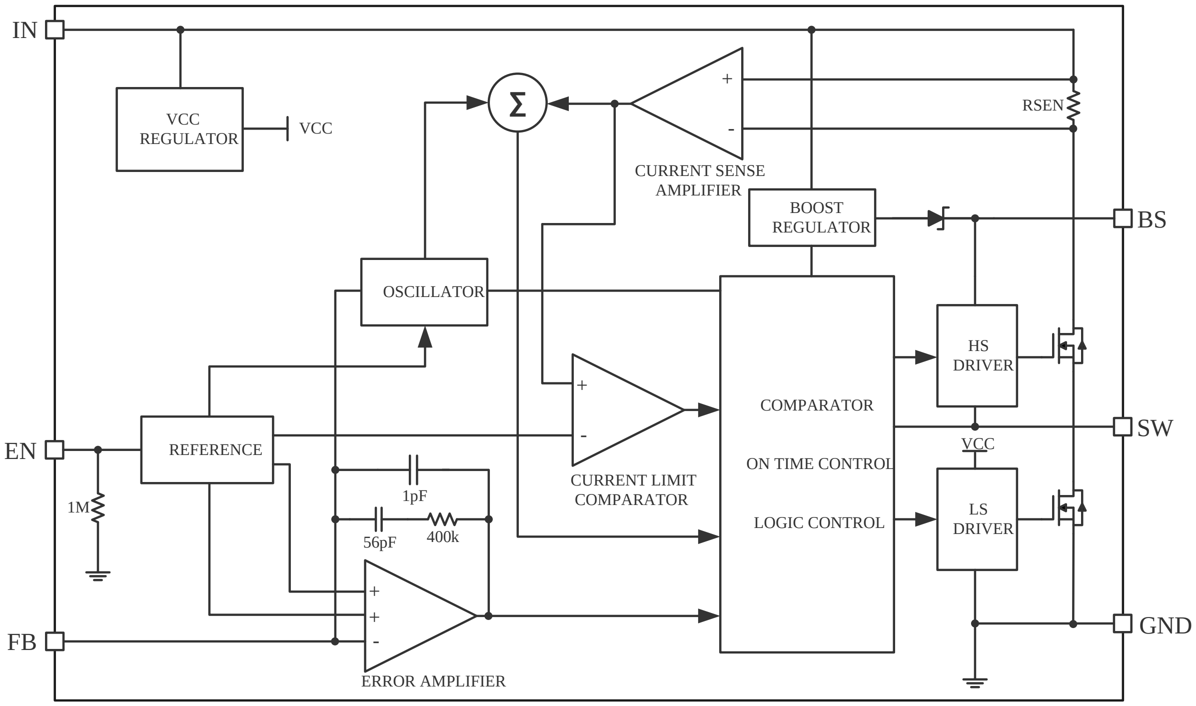


Figure2. FC6800 Block Diagram

Functional Description

Internal Regulator

The FC6800 is a current mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 600K operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal FB reference (V_{FB}) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current.The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Sof-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.6V. When it is lower than the internalreference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally fixed to 1 ms.

Over-Current-Protection and Hiccup

The FC6800 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 30% below the reference. Once a UV is triggered, the FC6800 enters hiccupmode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The FC6800 exits the hiccup mode once the over current condition is removed.

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Applications Information

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. Choose R1 to be around 100kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{FB}} - 1}$$

Inductor Selection

A 4.7µH to 22µH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ . For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current. Choose inductor ripple current to be approximately 30% if the maximum load current, 2A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency should be less than input source impedance to prevent high frequency switching current passing to the input. A low ESR input capacitor sized for maximum RMS current must be used. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 22µF ceramic capacitor for most applications is sufficient. A large value may be used for improved input voltage filtering.

Output Capacitor Selection

The output capacitor (C_{OUT}) is required to maintain the DC outputvoltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times L} \times \left(R_{ESR} + \frac{1}{8 \times f_{OSC} \times C_{OUT}} \right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{OSC}^{\ 2} \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The

FC6800 can be optimized for a wide range of capacitance and ESR values.

PCB Layout Recommendations

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines and take Figure3for reference.

- Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
- Bypass ceramic capacitors are suggested to be put close to the VINPin.
- Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
- V_{OUT}, SW away from sensitive analog areas such as FB.
- Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.
- An example of 2-layer PCB layout is shown in Figure 3 for reference.

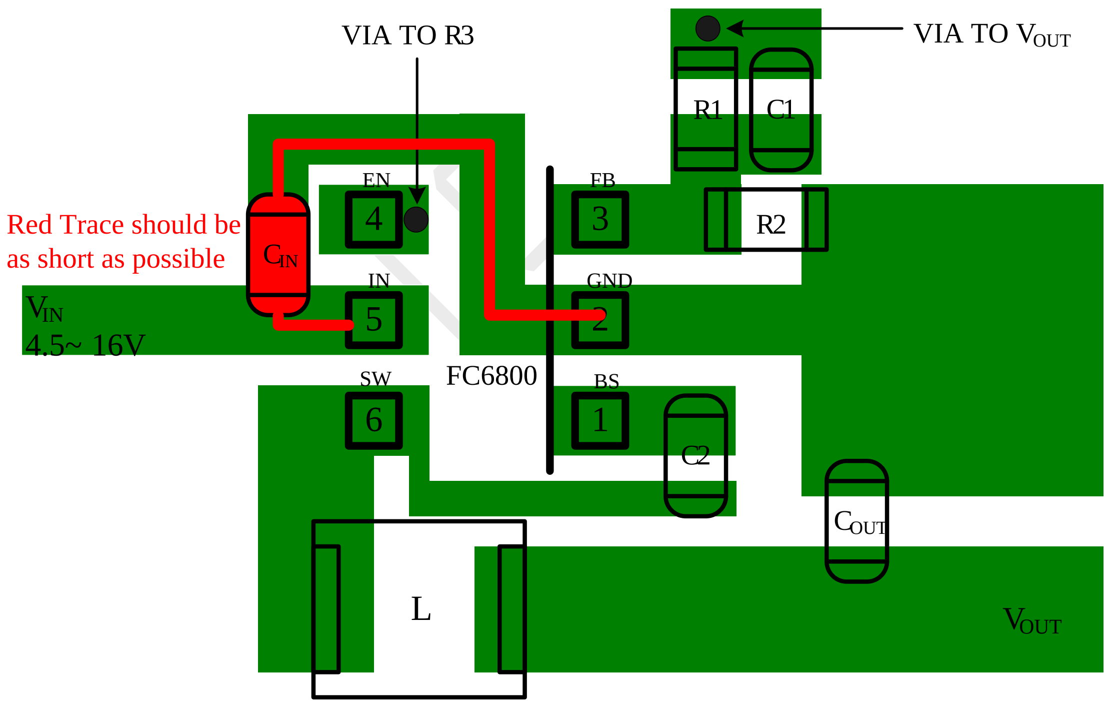
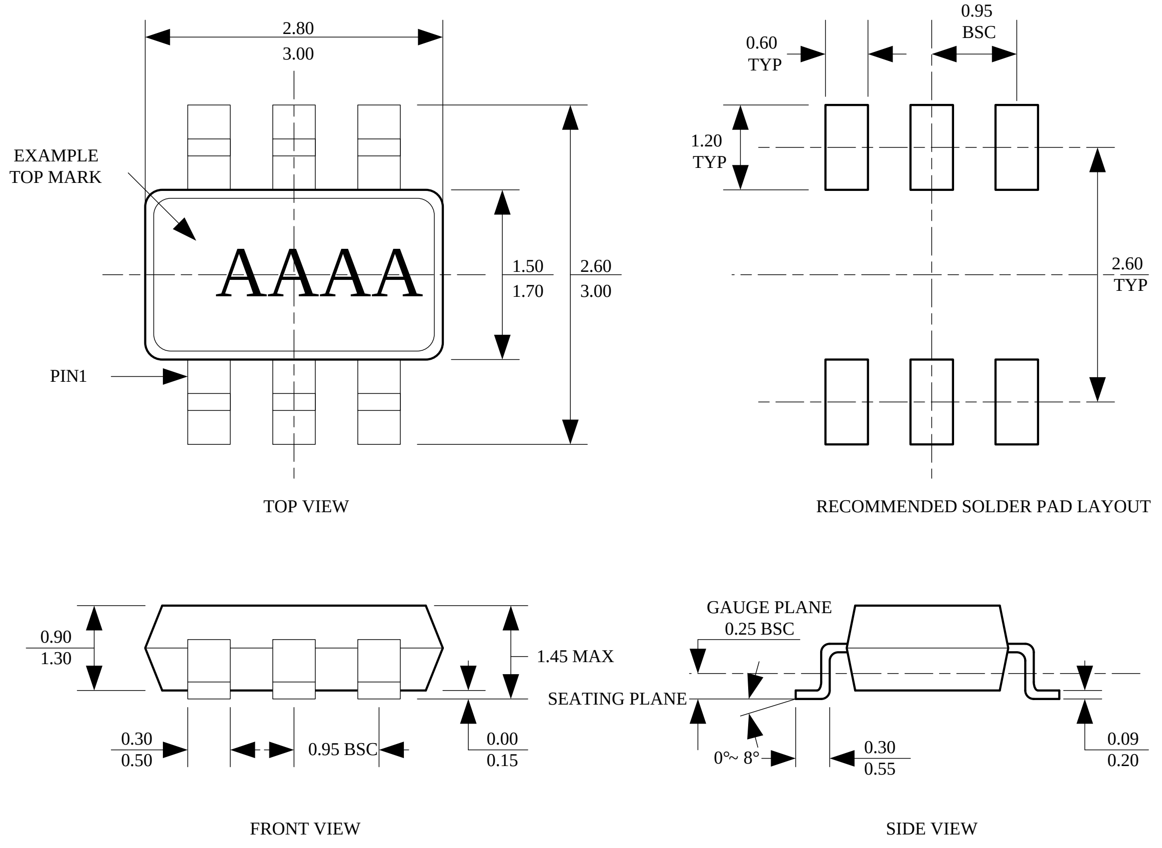


Figure3. FC6800 Suggested Layout

Package Description

SOT-23-6



NOTE
1.DIMENSIONS ARE IN MILLIMETERS
2.DRAWING NOT TO SCALE
3.DIMENSIONS ARE INCLUSIVE OF PLATING
4.DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR