

## Unity Power Factor LED Lamp Driver

### Features

- ▶ Constant output current
- ▶ Large step-down ratio
- ▶ Unity power factor
- ▶ Low input current harmonic distortion
- ▶ Fixed frequency or fixed off-time operation
- ▶ Internal 450V linear regulator
- ▶ Input and output current sensing
- ▶ Input current limit
- ▶ Enable, PWM and phase dimming

### Applications

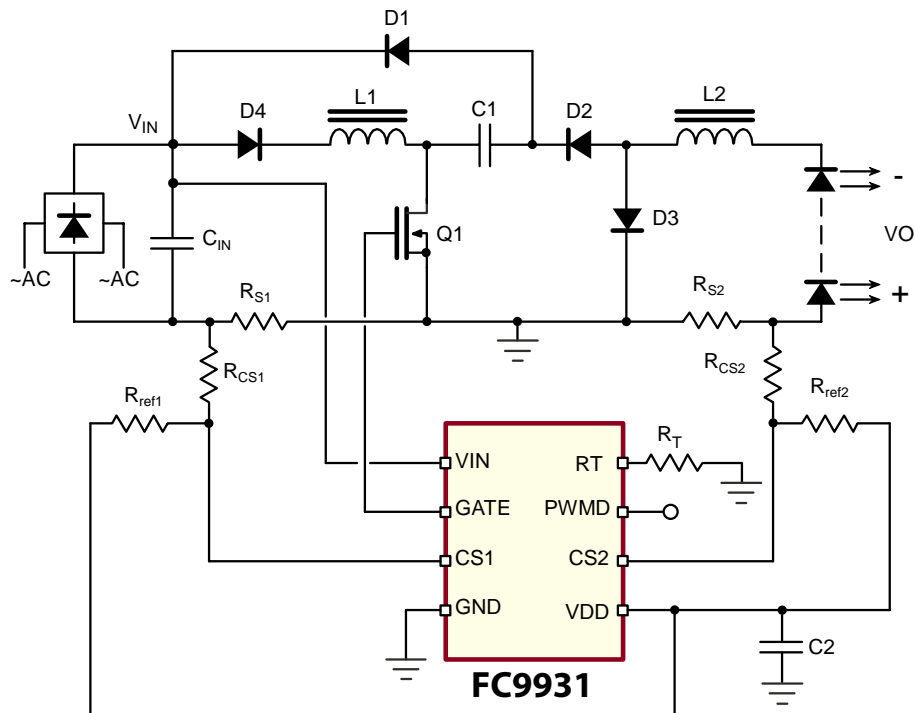
- ▶ Offline LED lamps and fixtures
- ▶ Street lamps
- ▶ Traffic signals
- ▶ Decorative lighting

### General Description

The FC9931 is a fixed frequency PWM controller IC designed to control an LED lamp driver using a single-stage PFC buckboost-buck topology. It can achieve a unity power factor and a very high step-down ratio that enables driving a single high-brightness LED from the 85-264VAC input without a need for a power transformer. This topology allows reducing the filter capacitors and using non-electrolytic capacitors to improve reliability. The FC9931 uses open-loop peak current control to regulate both the input and the output current. This control technique eliminates a need for loop compensation, limits the input inrush current, and is inherently protected from input under-voltage condition.

Capacitive isolation protects the LED Lamp from failure of the switching MOSFET. FC9931 provides a low-frequency PWM dimming input that can accept an external control signal with a duty ratio of 0-100% and a frequency of up to a few kilohertz. The PWM dimming capability enables FC9931 phase control solutions that can work with standard wall dimmers.

### Typical Application Circuit





## Absolute Maximum Ratings

V <sub>IN</sub> to GND	-----	-0.5V to +470V
V <sub>DD</sub> to GND	-----	-0.3V to +13,5V
CS1, CS2, PWM_D, GATE, RT to GND	-----	-0.3V to (V <sub>DD</sub> + 0.3V)
Operating Temperature Range	-----	-40°C to +85°C
Junction Temperature	-----	+125°C
Storage Temperature Range	-----	-65°C to +150°C
Continuous Power Dissipation (T <sub>a</sub> =+25°C) (Note 1)		
16-Pin SO (derate 7.5mW/°C above +25°C)	-----	750mW
8-Pin DIP (derate 9mW/°C above +25°C)	-----	900mW
8-Pin SO (derate 6.3mW/°C above +25°C)	-----	630mW

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Note1: Also limited by package power dissipation limit, whichever is lower.

## Electrical Characteristics (cont.) (The \* denotes the specifications which apply over the full operating junction temperature range of -40°C < T < +85°C, otherwise the specifications are at T = 25°C, V<sub>IN</sub>= 12V, unless otherwise noted)

Symbol	Description	Min	Typ	Max	Units	Conditions
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### Input

V <sub>INDC</sub>	Input DC supply voltage range*	8.0	-	450	V	DC input voltage
I <sub>INSD</sub>	Shut-Down mode supply current*	-	0.5	1	mA	Pin PWM_D to GND

### Internal Regulator

V <sub>DD</sub>	Internally regulated voltage	7.12	7.5	7.88	V	V <sub>IN</sub> = 8V, I <sub>DD(ext)</sub> =0, GATE = 500pF, R <sub>T</sub> = 226kΩ
ΔV <sub>DD,line</sub>	Line regulation of V <sub>DD</sub>	0	-	1.0	V	V <sub>IN</sub> = 8 - 450V, I <sub>DD(ext)</sub> = 0, GATE = 500pF, R <sub>T</sub> = 226kΩ
UVLO	V <sub>DD</sub> undervoltage lockout threshold	6.45	6.7	6.95	V	V <sub>IN</sub> rising
ΔUVLO	V <sub>DD</sub> undervoltage lockout hysteresis	-	500	-	mV	---

### PWM Dimming

V <sub>PWMD(lo)</sub>	PWM_D input low voltage			1.0	V	V <sub>IN</sub> = 8-450V
V <sub>PWMD(hi)</sub>	PWM_D input high voltage	2.4			V	V <sub>IN</sub> = 8-450V
R <sub>PWMD</sub>	PWM_D pull-down resistance	50	100	150	kΩ	V <sub>PWMD</sub> = 5V

### GATE

V <sub>GATE(hi)</sub>	GATE high output voltage*	V <sub>DD</sub> -0.3	-	V <sub>DD</sub>	V	I <sub>GATE</sub> = -10 mA, V <sub>DD</sub> = 7.5V, V <sub>IN</sub> open
V <sub>GATE(lo)</sub>	GATE low output voltage	0	-	0.3	V	I <sub>GATE</sub> = 10 mA V <sub>DD</sub> = 7.5V, V <sub>IN</sub> open
T <sub>RISE</sub>	GATE output rise time	-	30	50	ns	C <sub>GATE</sub> = 500pF, V <sub>DD</sub> = 7.5V, V <sub>IN</sub> open
T <sub>FALL</sub>	GATE output fall time	-	30	50	ns	C <sub>GATE</sub> = 500pF, V <sub>DD</sub> = 7.5V, V <sub>IN</sub> open
T <sub>DELAY</sub>	Delay from CS trip to GATE	-	150	300	ns	V <sub>CS1</sub> , V <sub>CS2</sub> = -100mV
T <sub>BLANK</sub>	Blanking delay	150	215	280	ns	V <sub>CS1</sub> , V <sub>CS2</sub> = -100mV

### Oscillator

F <sub>OSC</sub>	Oscillator frequency	80	100	120	kHz	R <sub>T</sub> = 226 kΩ
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### Comparators

T <sub>OFFSET1</sub> T <sub>OFFSET2</sub>	Comparator input offset voltage*	-15	-	15	mV	---
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## Functional Description

### Power Topology

The FC9931 is optimized to drive single-stage, single-switch, non-isolated topology, cascading an input power factor correction (PFC) buck-boost stage and an output buck converter power stage. This power converter topology offers numerous advantages useful for driving high-brightness light emitting diodes (HB LED). These advantages include unity power factor, low harmonic distortion of the input AC line current, and low output current ripple. The output load is decoupled from the input voltage with a capacitor making the driver inherently failure-safe for the output load. The power converter topology also permits reducing the size of a filter capacitor needed, enabling use of non-electrolytic capacitors. The latter advantage greatly improves reliability of the overall solution.

The FC9931 is a peak current-mode controller that is specifically designed to drive a constant current buck-boost-buck power converter. This patent pending control scheme features two identical current sense comparators for detecting negative current signal levels. One of the comparators regulates the output LED current, while the other is used for sensing the input inductor current. The second comparator is mainly responsible for the converter start-up. The control scheme inherently features low inrush current and input under-voltage protection. The FC9931 can operate with programmable constant frequency or constant off-time. In many cases, the constant off-time operating mode is preferred, since it improves line regulation of the output current, reduces voltage stress of the power components and simplifies regulatory EMI compliance.

### Input Voltage Regulator

The FC9931 can be powered directly from its VIN pin, and takes a voltage from 8V to 450V. When a voltage is applied at the VIN pin, the FC9931 seeks to maintain a constant 7.5V at the VDD pin. The  $V_{DD}$  voltage can be also used as a reference for the current sense comparators. The regulator is equipped with an under-voltage protection circuit which shuts off the FC9931 when the voltage at the VDD pin falls below 6.2V.

The VDD pin must be bypassed by a low ESR capacitor ( $\geq 0.1\mu\text{F}$ ) to provide a low impedance path for the high frequency current of the output GATE driver.

The FC9931 can also be operated by supplying a voltage at the VDD pin greater than the internally regulated voltage. This will turn off the internal linear regulator and the FC9931 will function by drawing power from the external voltage source connected to the VDD pin.

### PWM Dimming and Wall Dimmer Compatibility

PWM Dimming can be achieved by applying a TTL-compatible square wave signal at the PWMD pin. When the PWMD pin is pulled high, the GATE driver is enabled and the circuit operates normally. When the PWMD pin is left open or connected to GND, the GATE driver is disabled and the external MOSFET turns off. The FC9931 is designed so that the signal at the PWMD pin inhibits the driver only, and the IC need not go through the entire start-up cycle each time ensuring a quick response time for the output current.

The power topology requires little filter capacitance at the output, since the output current of the buck stage is continuous, and since AC line filtering is accomplished through the middle capacitor rather than the output one. Therefore, disabling the FC9931 via its PWMD or VIN pins can interrupt the output LED current in accordance with the phase-controlled voltage waveform of a standard wall dimmer.

### Oscillator

Connecting an external resistor from RT pin to GND programs switching frequency:

$$F_s [kHz] = \frac{25000}{R_T [K\Omega] + 22}$$

Connecting the resistor from the RT pin to the GATE programs constant off-time:

$$T_{OFF} [\mu s] = \frac{R_T [K\Omega] + 22}{25}$$

## Input and Output Current Feedback

Two current sense comparators are included in the FC9931. Both comparators have their non-inverting inputs internally connected to ground (GND). The CS1 and CS2 inputs are inverting inputs of the comparators. Connecting a resistor divider into either of these inputs from a positive reference voltage and a negative current sense signal programs the current sense threshold of the comparator. The  $V_{DD}$  voltage of the FC9931 can be used as the reference voltage. If more accuracy is needed, an external reference voltage can be applied. When either the CS1 or the CS2 pin voltage falls below GND, the GATE pulse is terminated. A leading edge blanking delay of 215ns (typ) is added. The GATE voltage becomes high again upon receiving the next clock pulse of the oscillator circuit.

Referring to the Functional Circuit Diagram, the CS2 comparator is responsible for regulating output current. The output LED current can be programmed using the following equation:

$$R_{CS2} = \frac{I_O + \frac{1}{2} \Delta I_{L2}}{7.5V} \cdot R_{REF2} \cdot R_{S2}$$

where  $\Delta I_{L2}$  is the peak-to-peak current ripple in L2. The CS1 comparator limits the current in the input inductor L1. There is no charge in the capacitor C1 upon the start-up of the converter. Therefore, L2 cannot develop the output current, and the FC9931 starts-up in the input current limiting mode. The CS1 current threshold must be programmed such that no input current limiting occurs in normal steady-state operation. The CS1 threshold can be programmed in accordance with a similar equation:

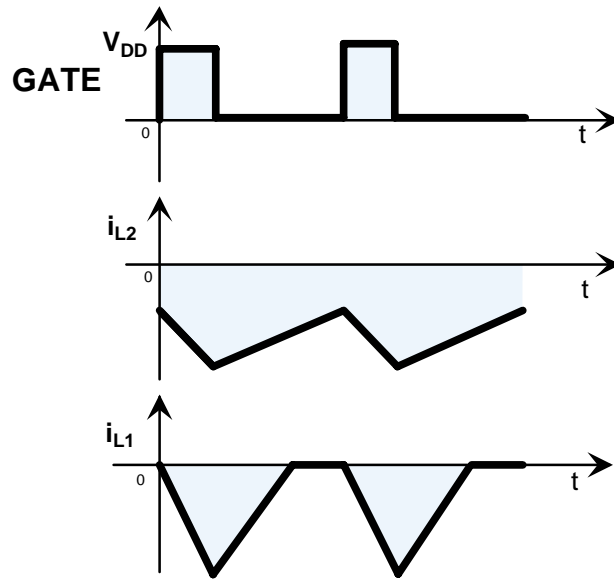
$$R_{CS1} = \frac{I_{L1(PK)}}{7.5V} \cdot R_{REF1} \cdot R_{S1}$$

where  $I_{L1(PK)}$  is the maximum peak current in L1.

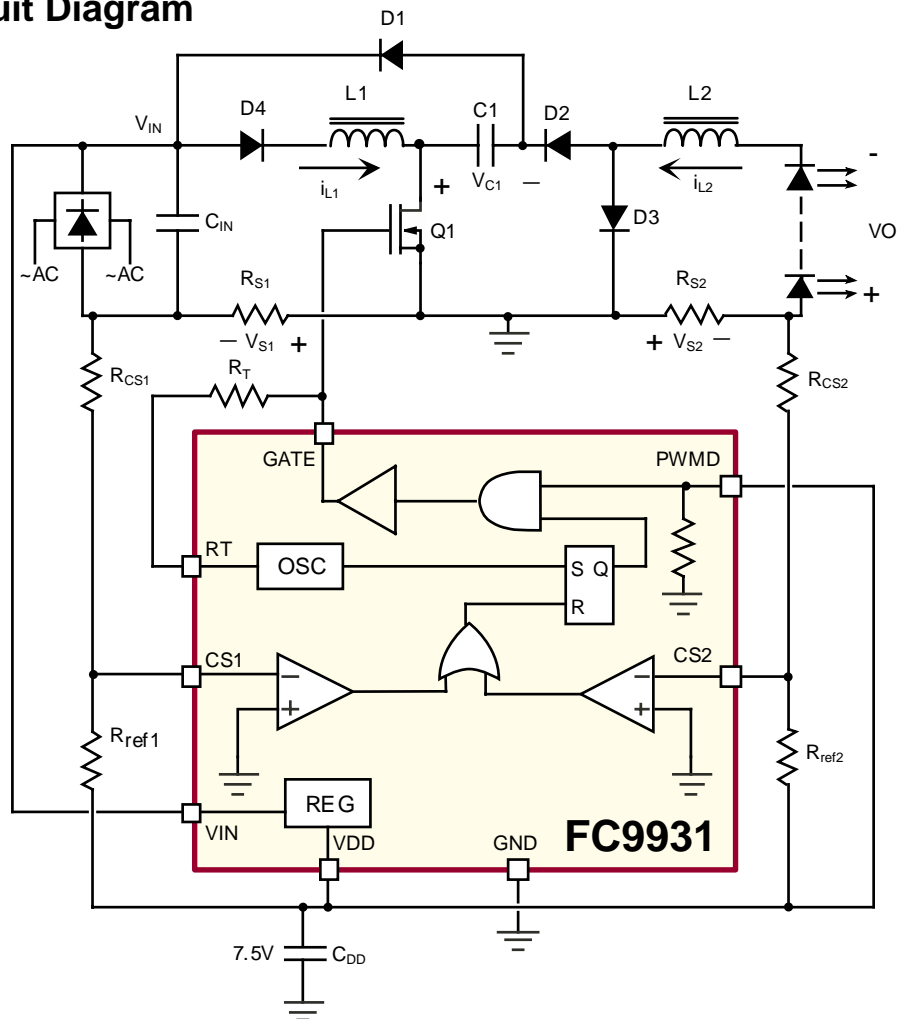
## MOSFET Gate Driver

Typically, the GATE driving capability of the FC9931 is limited by the amount of power dissipation in its linear regulator. Thus, care must be taken selecting a switching MOSFET to be used in the circuit. An optimal trade-off must be found between the GATE charge and the on-resistance of the MOSFET to minimize the input regulator current.

## Switching Waveform

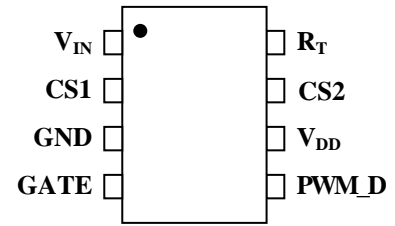


## Functional Circuit Diagram

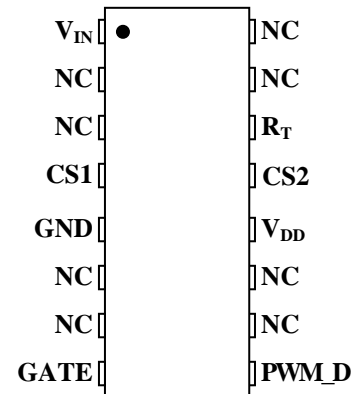


## Pinout

Name	SO-16	SO-8 DIP-8	Description
V <sub>IN</sub>	1	1	This pin is the input of a high voltage regulator.
CS1	4	2	This pin is used to sense the input and output currents of the converter. It is the inverting input of the internal comparator.
GND	5	3	Ground return for all the internal circuitry. This pin must be electrically connected to the ground of the power train.
GATE	8	4	This pin is the output GATE driver for an external N-channel power MOSFET
PWM_D	9	5	When this pin is pulled to GND, switching of the FC9931 is disabled. When the PWMD pin is released, or external TTL high level is applied to it, switching will resume. This feature is provided for applications that require PWM dimming of the LED lamp.
V <sub>DD</sub>	12	6	This is a power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND.
CS2	13	7	This pin is used to sense the input and output currents of the converter. It is the inverting input of the internal comparator.
R <sub>T</sub>	14	8	Oscillator control. A resistor connected between this pin and GND sets the PWM frequency. A resistor connected between this pin and GATE sets the PWM off-time.



8-Pin DIP/SOIC



16-Pin SOIC

No Connects (NC) are not internally connected and may be used for pass-thru PCB traces