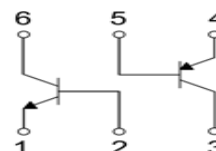


Plastic-Encapsulate Transistors

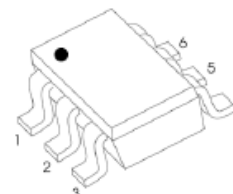
DUAL TRANSISTOR (NPN+PNP)



FEATURES

- Epitaxial Die Construction
- Two isolated NPN/PNP(BC817W+BC807W) Transistors in one package

MAKING: 56B



SOT23-6L

MAXIMUM RATINGS TR1 ($T_a=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage	50	V
V_{CEO}	Collector-Emitter Voltage	45	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current -Continuous	0.5	A
P_C	Collector Dissipation	0.2	W
$R_{\theta JA}$	Thermal Resistance from Junction to Ambient	625	$^{\circ}\text{C/W}$
T_j	Junction Temperature	150	$^{\circ}\text{C}$
T_{stg}	Storage Temperature	-55~+150	$^{\circ}\text{C}$

CHARACTERISTICS of TR1 (NPN Transistor) ($T_a=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Collector-base breakdown voltage	$V_{(BR)CBO}$	$I_C=10\mu\text{A}, I_E=0$	50			V
Collector-emitter breakdown voltage	$V_{(BR)CEO}$	$I_C=10\text{mA}, I_B=0$	45			V
Emitter-base breakdown voltage	$V_{(BR)EBO}$	$I_E=1\mu\text{A}, I_C=0$	5			V
Collector cut-off current	I_{CBO}	$V_{CB}=20\text{V}, I_E=0$			0.1	μA
Emitter cut-off current	I_{EBO}	$V_{EB}=5\text{V}, I_C=0$			0.1	μA
DC current gain	$h_{FE(1)}$	$V_{CE}=1\text{V}, I_C=100\text{mA}$	160		400	
	$h_{FE(2)}$	$V_{CE}=1\text{V}, I_C=500\text{mA}$	40			
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C=500\text{mA}, I_B=50\text{mA}$			0.7	V
Base-emitter saturation voltage	$V_{BE(sat)}$	$I_C=500\text{mA}, I_B=50\text{mA}$			1.2	V
Base-emitter voltage	$V_{BE(ON)}$	$V_{CE}=1\text{V}, I_C=500\text{mA}$			1.2	V
Transition frequency	f_T	$V_{CE}=5\text{V}, I_C=10\text{mA}, f=100\text{MHz}$	100			MHz
Collector output capacitance	C_{ob}	$V_{CB}=10\text{V}, f=1\text{MHz}$			5	pF

MAXIMUM RATINGS TR2 ($T_a=25^{\circ}\text{C}$ unless otherwise noted)

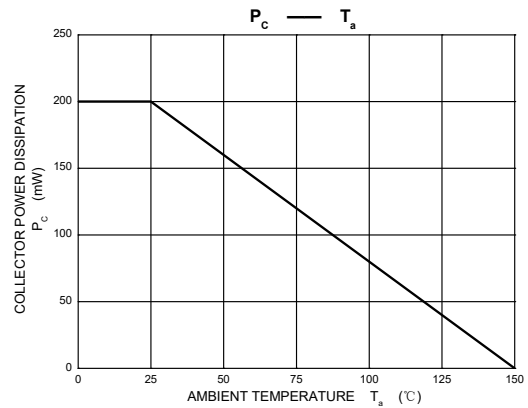
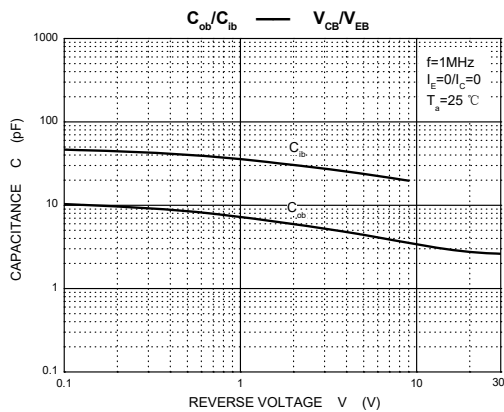
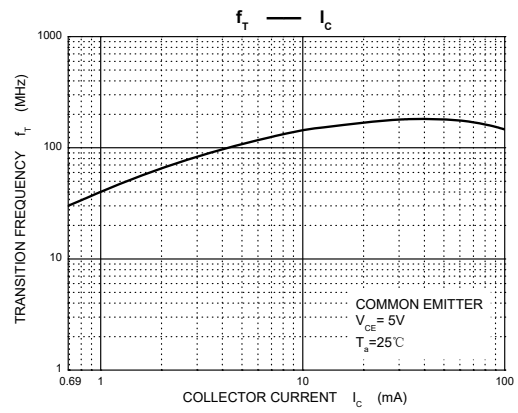
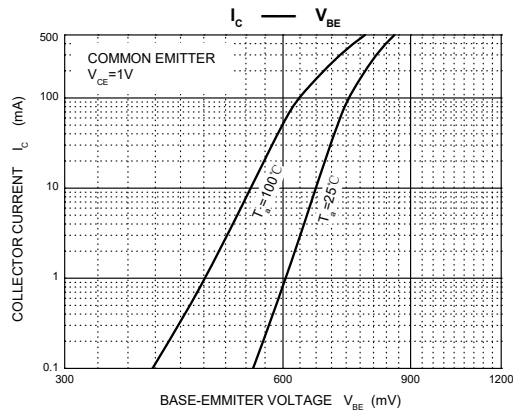
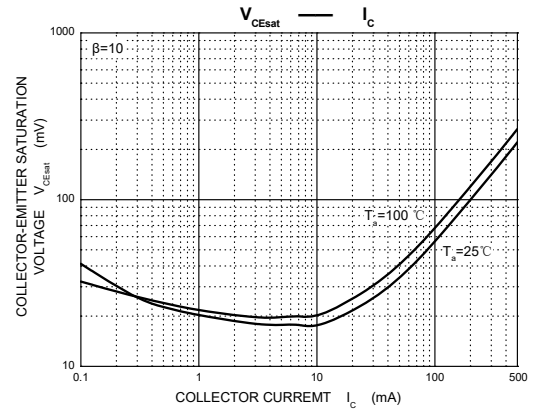
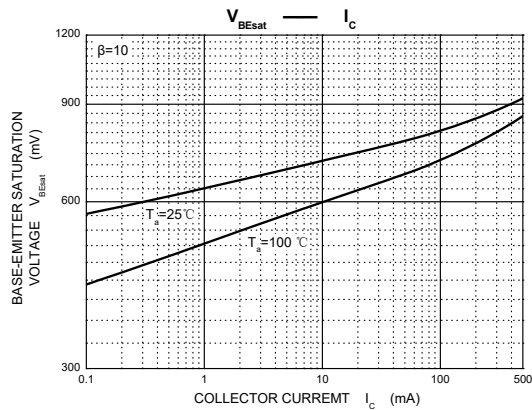
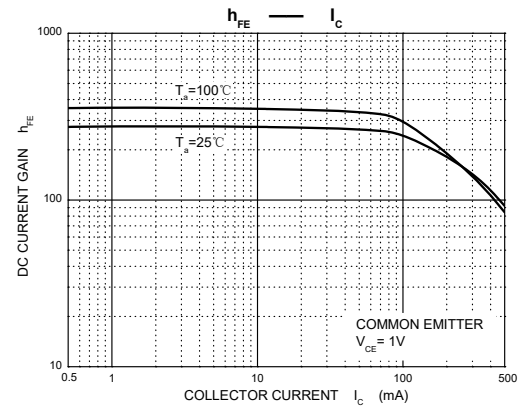
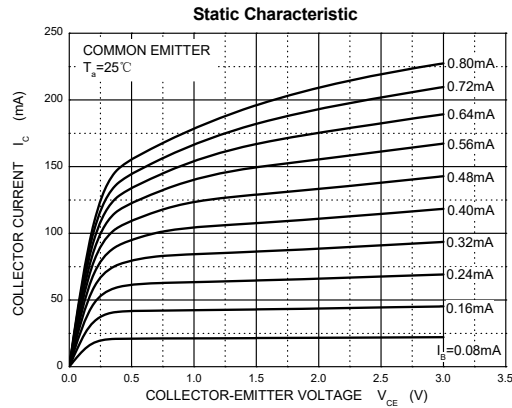
Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage	-50	V
V_{CEO}	Collector-Emitter Voltage	-45	V
V_{EBO}	Emitter-Base Voltage	-5	V
I_C	Collector Current	-500	mA
P_C	Collector Power Dissipation	200	mW
$R_{\theta JA}$	Thermal Resistance From Junction To Ambient	417	$^{\circ}\text{C/W}$
T_j	Junction Temperature	150	$^{\circ}\text{C}$
T_{stg}	Storage Temperature	-55 ~ +150	$^{\circ}\text{C}$

CHARACTERISTICS of TR2 (PNP Transistor) ($T_a=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test conditions	Min	Max	Unit
Collector-base breakdown voltage	V_{CBO}	$I_C=-10\mu\text{A}, I_E=0$	-50		V
Collector-emitter breakdown voltage	V_{CEO}	$I_C=-10\text{mA}, I_B=0$	-45		V
Emitter-base breakdown voltage	V_{EBO}	$I_E=-1\mu\text{A}, I_C=0$	-5		V
Collector cut-off current	I_{CBO}	$V_{CB}=-20\text{ V}, I_E=0$		-0.1	μA
Collector cut-off current	I_{CEO}	$V_{CE}=-20\text{ V}, I_B=0$		-0.2	μA
Emitter cut-off current	I_{EBO}	$V_{EB}=-5\text{ V}, I_C=0$		-0.1	μA
DC current gain	$h_{FE(1)}$	$V_{CE}=-1\text{V}, I_C=-100\text{mA}$	160	400	
	$h_{FE(2)}$	$V_{CE}=-1\text{V}, I_C=-500\text{mA}$	40		
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C=-500\text{mA}, I_B=-50\text{ mA}$		-0.7	V
Base-emitter voltage	$V_{BE(on)}$	$V_{CE}=-1\text{V}, I_C=-500\text{mA}$		-1.2	V
Transition frequency	f_T	$V_{CE}=-5\text{ V}, I_C=-10\text{mA}$ $f=100\text{MHz}$	80		MHz
Collector output capacitance	C_{ob}	$V_{CB}=-10\text{V}, f=1\text{MHz}$		10	pF

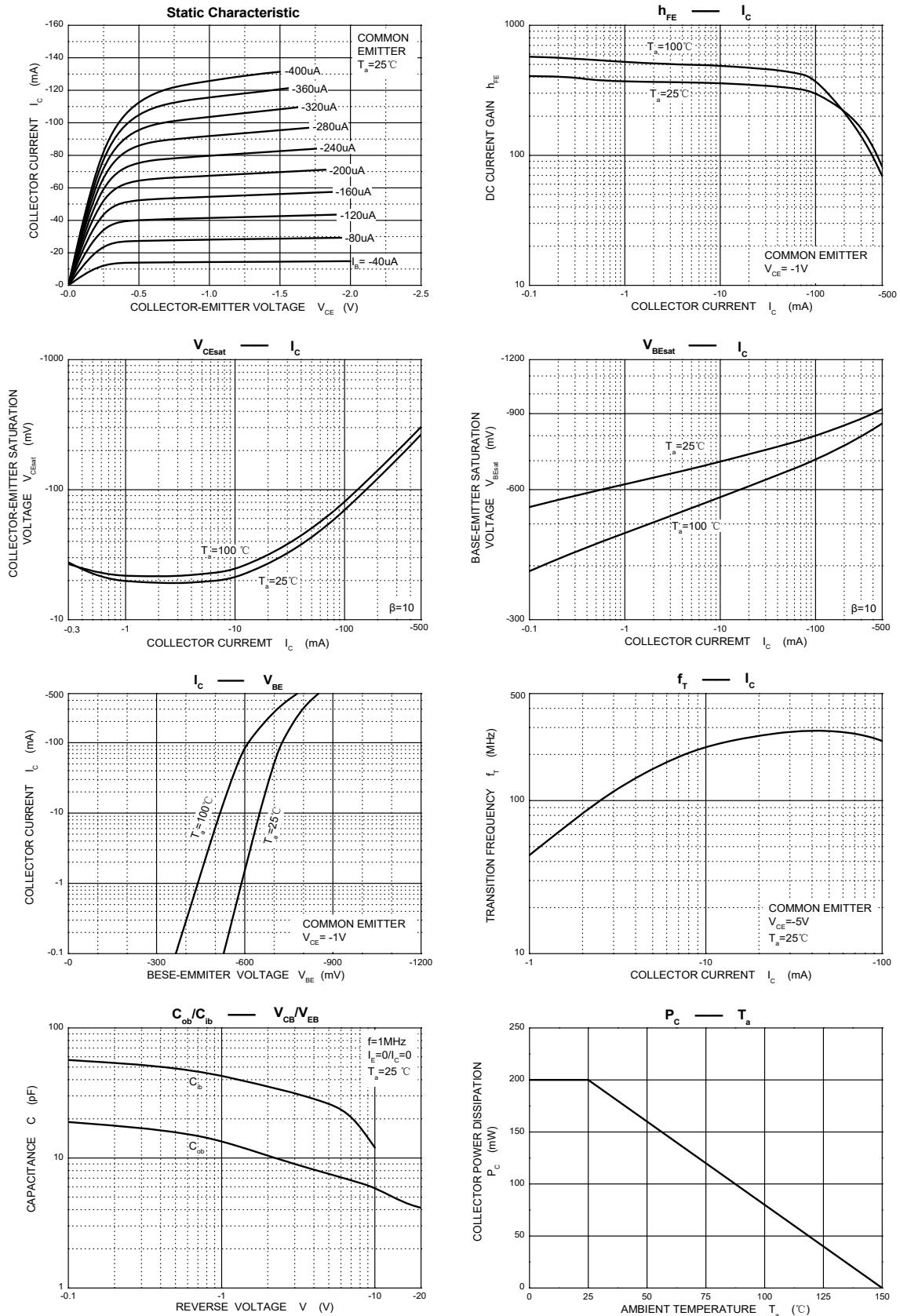
Typical Characteristics

BC817DPN/TR1

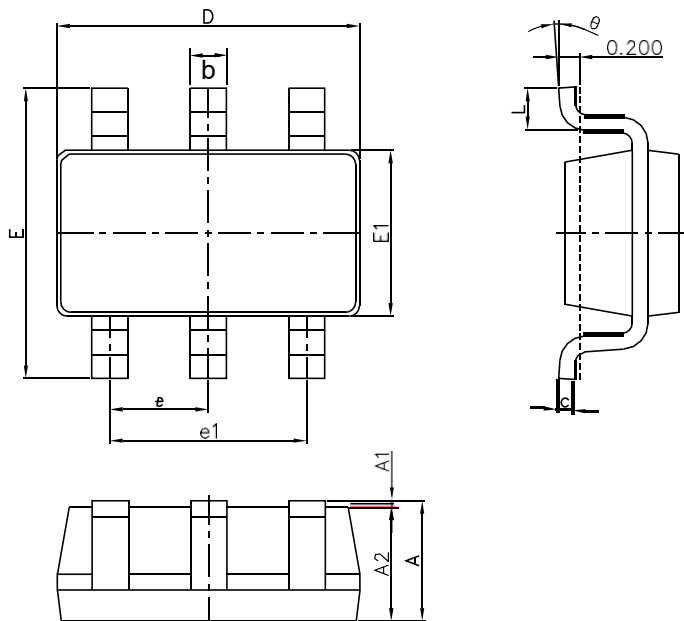


Typical Characteristics

BC807DPN/TR2

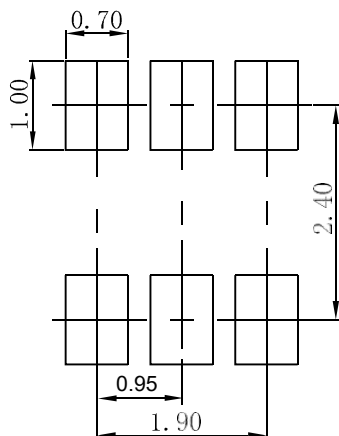


SOT-23-6L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT-23-6L Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.