

N-Channel Power MOSFET

GENERAL DESCRIPTION

This advanced high voltage MOSFET is designed to stand high energy in the avalanche mode and switch efficiently.

This new high energy device also offers a drain

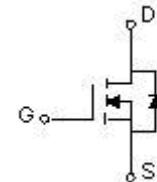
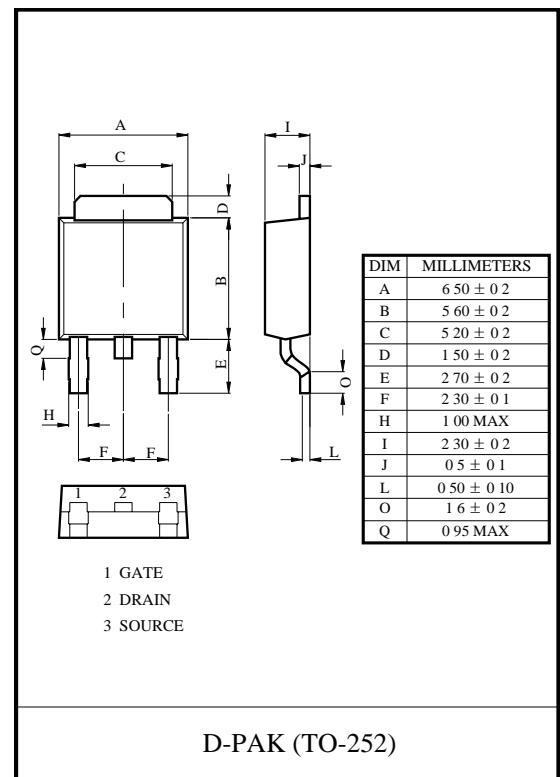
Designed for high voltage, high speed power supplies , converters, power motor controls and bridge circuits power supplies

FEATURE

- High density cell design for ultra low $R_{ds(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

APPLICATION

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



MAXIMUM RATINGS ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	40	A
Pulsed Drain Current	I_{DM}	160	A
Single Pulsed Avalanche Energy	$E_{AS}^{(1)}$	320	mJ
Power Dissipation ($T_A=25^\circ\text{C}$)	P_D	1.25	W
Power Dissipation ($T_c=25^\circ\text{C}$)	P_D	102	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	100	°C/W
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	-55 ~+150	°C
Lead Temperature for Soldering Purposes(1/8" from case for 10s)	T_L	260	°C

(1). E_{AS} condition: $V_{DD}=50\text{V}$, $L=0.5\text{mH}$, $R_G=25\Omega$, Starting $T_J = 25^\circ\text{C}$



FTK40N10D

ELECTRICAL CHARACTERISTICS($T_a=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	100			V
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}} = 100\text{V}, V_{\text{GS}} = 0\text{V}$			1	μA
Gate-body leakage current	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 20\text{V}$			± 100	nA
On characteristics (note1)						
Gate-threshold voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	2		4	V
Static drain-source on-state resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 28\text{A}$		14	17	$\text{m}\Omega$
Forward transconductance	g_{fs}	$V_{\text{DS}} = 25\text{V}, I_D = 28\text{A}$	32			S
Dynamic characteristics (note 2)						
Input capacitance	C_{iss}	$V_{\text{DS}} = 30\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$		3400		pF
Output capacitance	C_{oss}			290		
Reverse transfer capacitance	C_{rss}			221		
Switching characteristics (note 2)						
Total gate charge	Q_g	$V_{\text{DS}} = 30\text{V}, V_{\text{GS}} = 10\text{V}, I_D = 30\text{A}$		94		nC
Gate-source charge	Q_{gs}			16		
Gate-drain charge	Q_{gd}			24		
Turn-on delay time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 30\text{V}, V_{\text{GS}} = 10\text{V}, R_G = 2.5\Omega, I_D = 2\text{A}, R_L = 15\Omega$		15		ns
Turn-on rise time	t_r			11		
Turn-off delay time	$t_{\text{d}(\text{off})}$			52		
Turn-off fall time	t_f			13		
Drain-Source Diode Characteristics						
Drain-source diode forward voltage(note1)	V_{SD}	$V_{\text{GS}} = 0\text{V}, I_S = 28\text{A}$			1.2	V
Continuous drain-source diode forward current	I_S				40	A
Pulsed drain-source diode forward current	I_{SM}				160	A

Notes:

1. Pulse Test : Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production.

Typical Electrical and Thermal Characteristics (Curves)

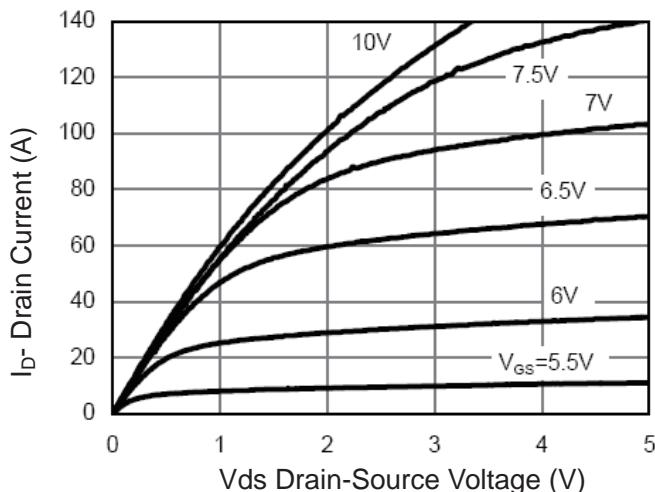


Figure 1 Output Characteristics

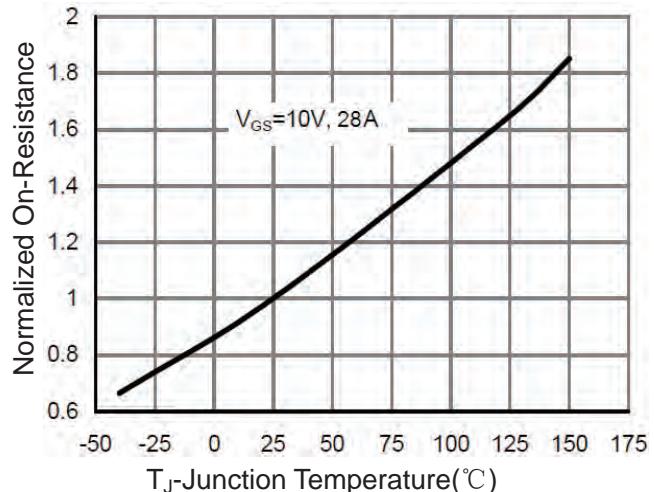


Figure 4 Rdson-JunctionTemperature

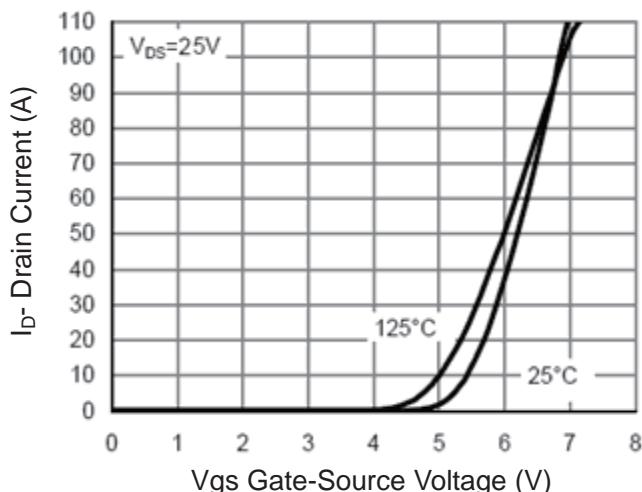


Figure 2 Transfer Characteristics

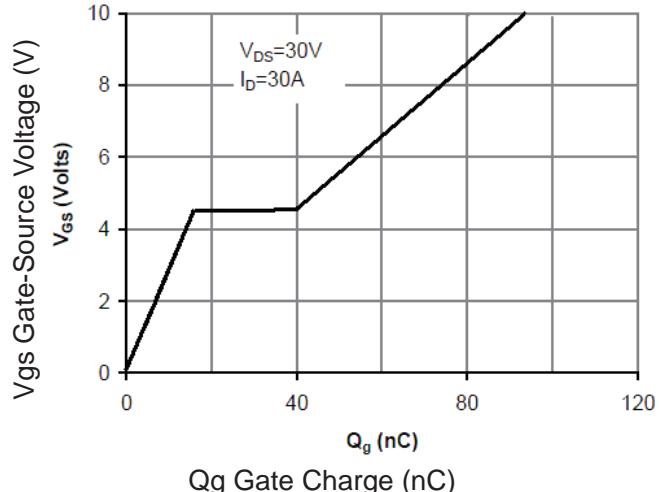


Figure 5 Gate Charge

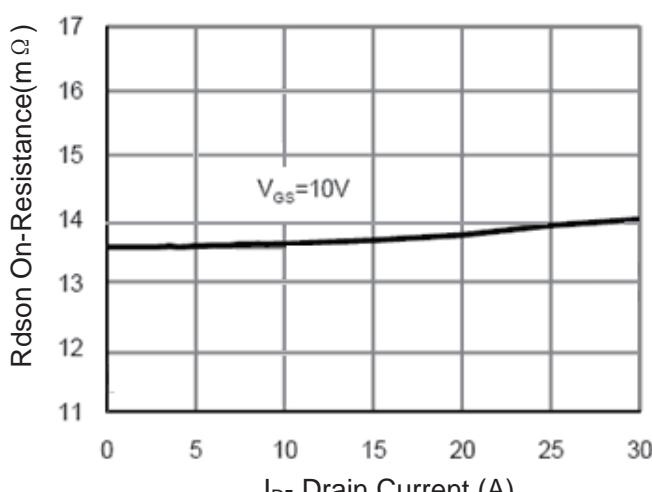


Figure 3 Rdson- Drain Current

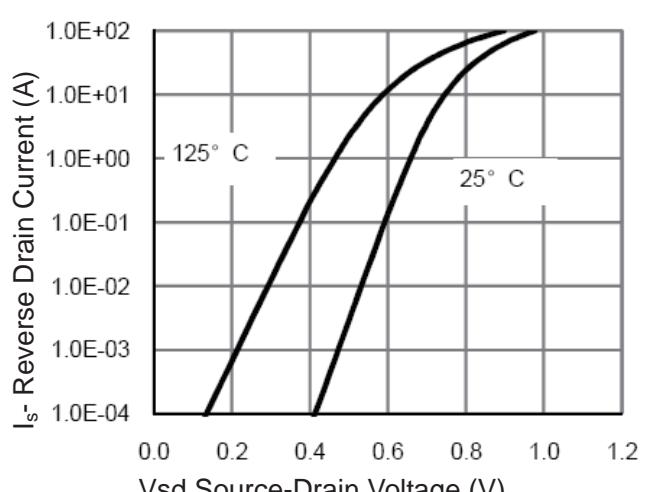
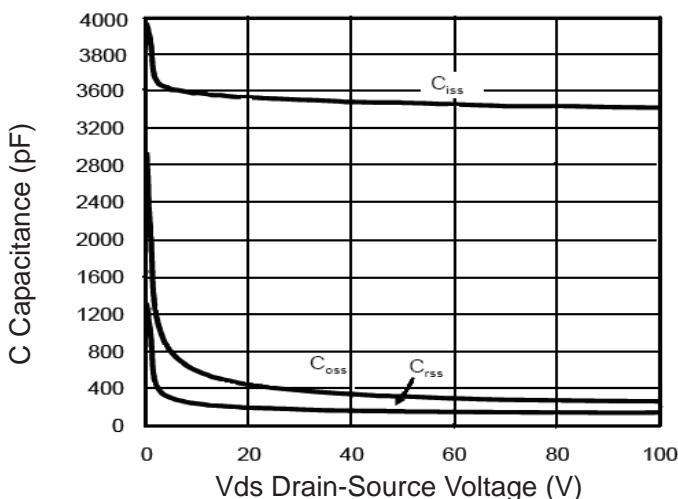
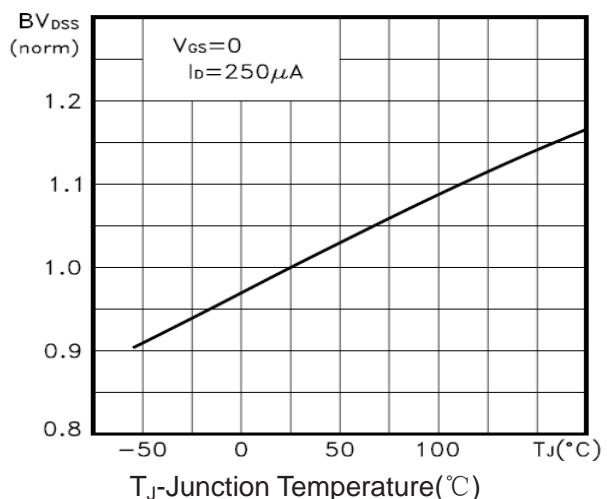
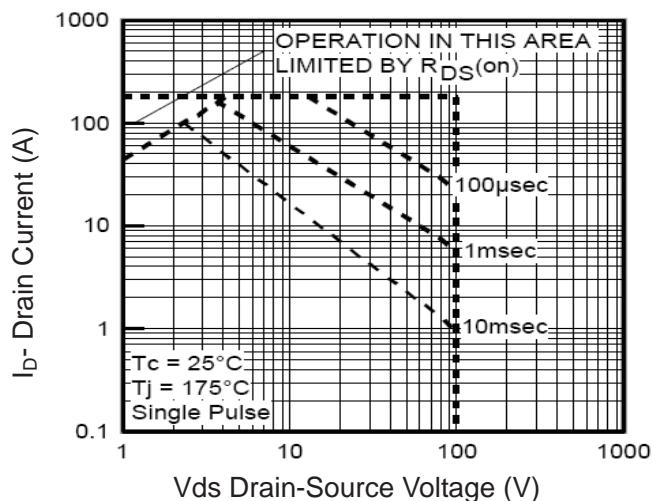
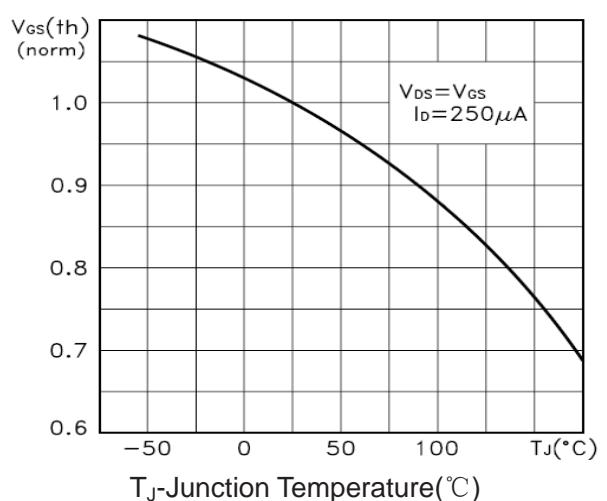
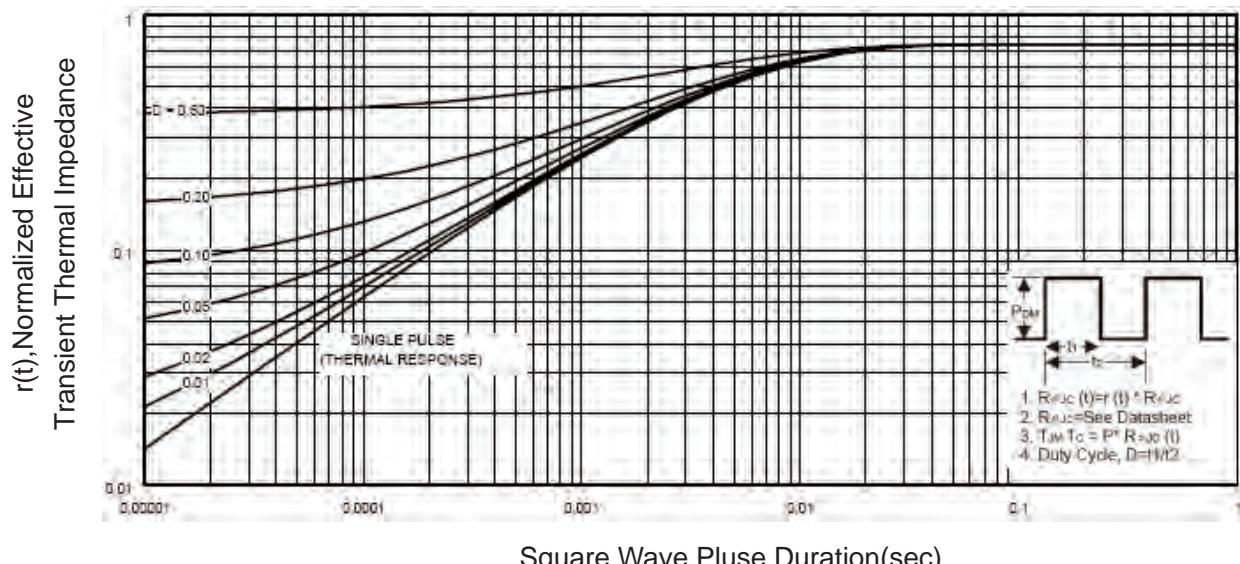


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 BV_{dss} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 $V_{GS(\text{th})}$ vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance