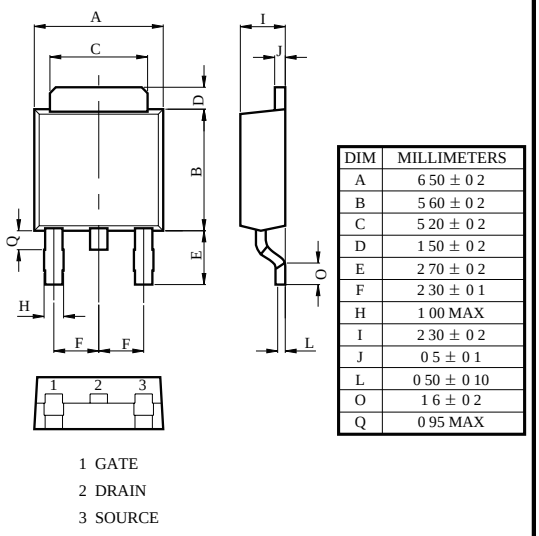
FTK55P30D P-Channel Power MOSFET



DIM	MILLIMETERS
A	6 50 ± 0 2
B	5 60 ± 0 2
C	5 20 ± 0 2
D	1 50 ± 0 2
E	2 70 ± 0 2
F	2 30 ± 0 1
H	1 00 MAX
I	2 30 ± 0 2
J	0 5 ± 0 1
L	0 50 ± 0 10
O	1 6 ± 0 2
Q	0 95 MAX

1 GATE
2 DRAIN
3 SOURCE

D-PAK (TO-252)

DESCRIPTION

The FTK55P30D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge.

This device is well suited for high current load applications.

FEATURES

- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
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APPLICATIONS

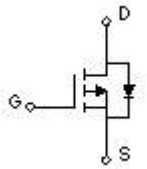
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible Power Supply

MARKING

NCE55P30K= Part No.

XXXX=Date Code

EQUIVALENT CIRCUIT



MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain- Source Voltage	V_{DS}	- 55	V
Gate- Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	- 30	A
Pulsed Drain Current	I_{DM}	- 120	A
Single Pulsed Avalanche Energy	E_{AS}(1)	225	mJ
Power Dissipation	$P_{D\ (Tc=25℃)}$	65	W
(Note 4a)	$P_{D\ (Ta=25℃)}$	2.2	W
Thermal Resistance from Junction to Ambient	$R_{\Theta JA}$	56	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature Range	T_{stg}	- 55 ~ +150	℃
Lead Temperature for Soldering Purposes(1/8'' from case for 10s)	T_L	260	℃

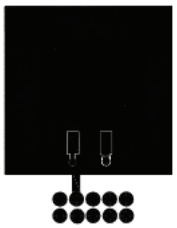
(1) E_{AS} condition: V_{DD}=- 25V,L=0.5mH, R_G=25Ω, Starting T_J = 25°C

Electrical characteristics (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	V_{GS} = 0V, I_D=-250μA	-55			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-55V, V_{GS}=0V			-1	μA
Gate-body leakage current	I_{GSS}	V_{DS} =0V, V_{GS} =±20V			±100	nA
On characteristics (note1)						
Gate - threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D=-250μA	-2.0		-4	V
Static drain-source on-sate resistance	$R_{DS(on)}$	V_{GS} =-10V, I_D=-15A			40	mΩ
Forward transconductance	g_{FS}	V_{DS} =-25V, I_D=-16A	8			S
Dynamic characteristics (note 2)						
Input capacitance	C_{iss}	V_{DS} =-30V,V_{GS}=0V, f =1MHz		3500		pF
Output capacitance	C_{oss}			240		
Reverse transfer capacitance	C_{rss}			153		
Switching characteristics (note 2)						
Total gate charge	Q_g	V_{DS}=-30V, V_{GS}=-10V, I_D=-15A		56		nC
Gate- source charge	Q_{gs}			11		
Gate - drain charge	Q_{gd}			24		
Turn-on delay time	$t_{d(on)}$	V_{DD}=-30V, I_D=-15A V_{GS}=-10V,R_G=3Ω,		12		ns
Turn-on rise time	t_r			15		
Turn-off delay time	$t_{d(off)}$			38		
Turn-off fall time	t_f			15		
Drain-Source Diode Characteristics						
Drain-source diode forward voltage(note1)	V_{SD}	V_{GS} =0V, I_S =-24A			-1.2	V
Continuous drain-source diode forward current (note3)	I_S				-30	A
Pulsed drain-source diode forward current	I_{SM}				-120	A

Notes:

1. Pulse Test : Pulse Width≤300μs, duty cycle ≤2%.
2. Guaranteed by design, not subject to production.
3. Surface Mounted on FR4 Board, t≤10 sec.
4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.
   $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

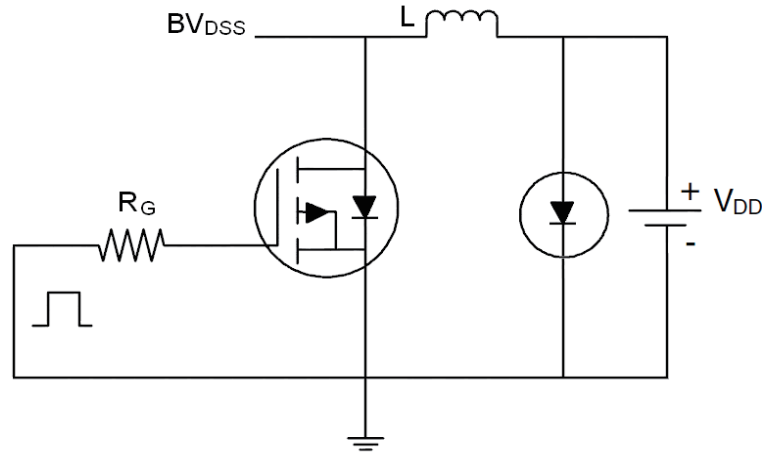


a) 52°C/W when mounted on a 1 in^2 pad of 2 oz copper

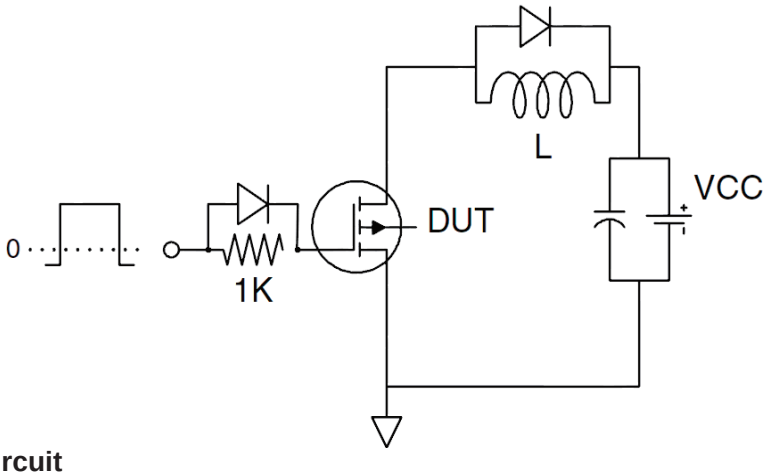
b) 100°C/W when mounted on a minimum pad.

Test Circuit

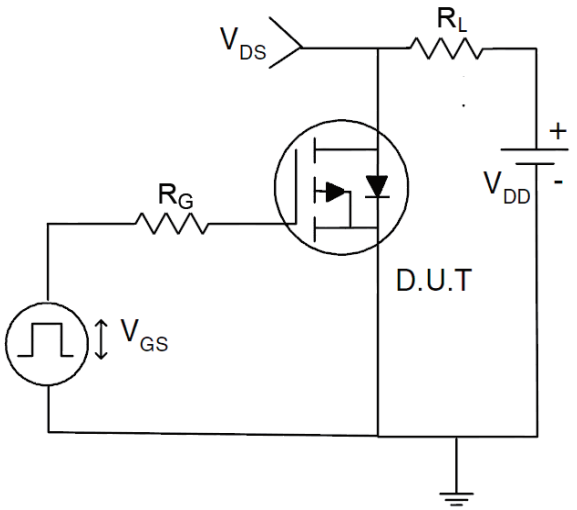
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (curves)

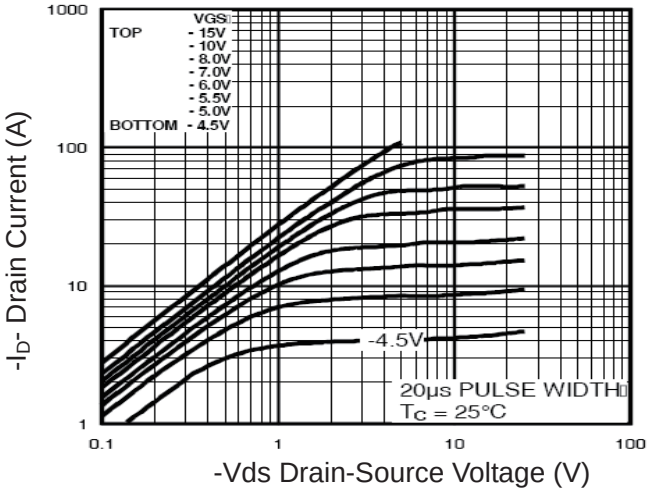


Figure 1 Output Characteristics

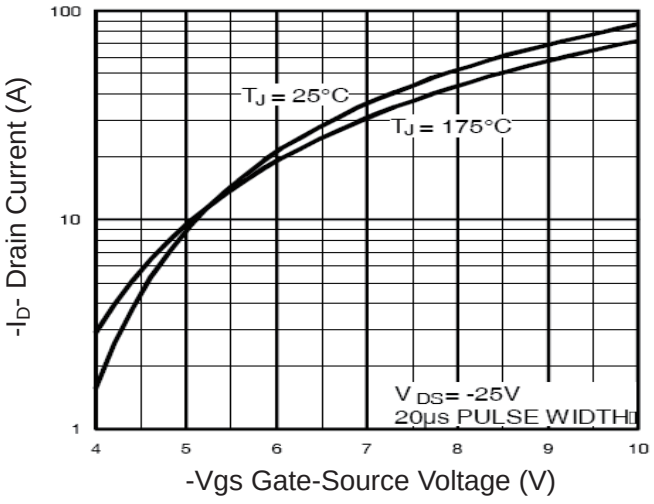


Figure 2 Transfer Characteristics

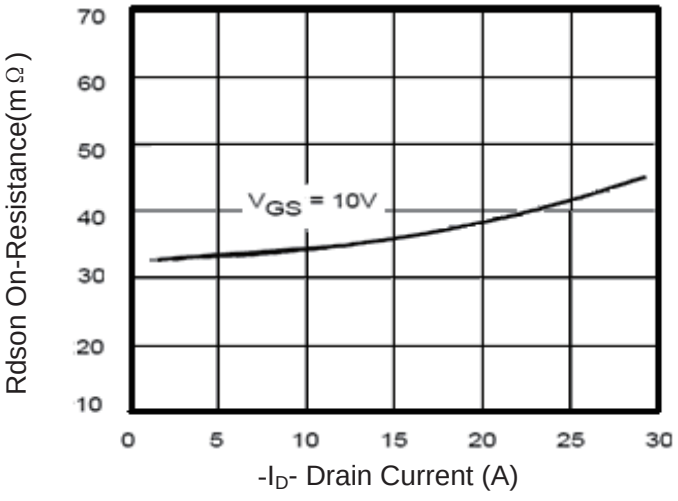


Figure 3 Rdson- Drain Current

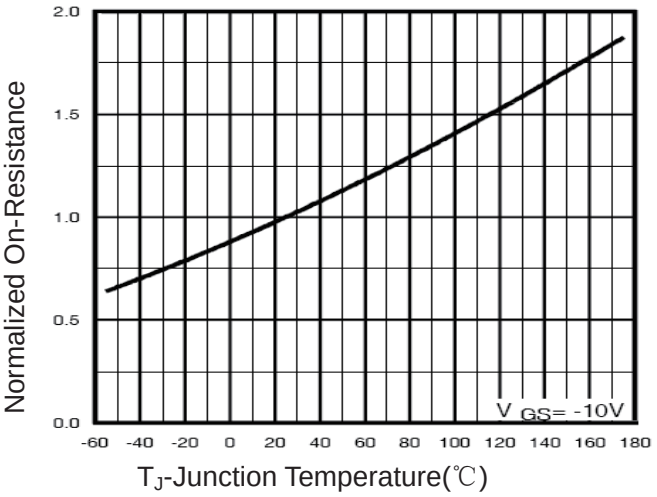


Figure 4 Rdson-JunctionTemperature

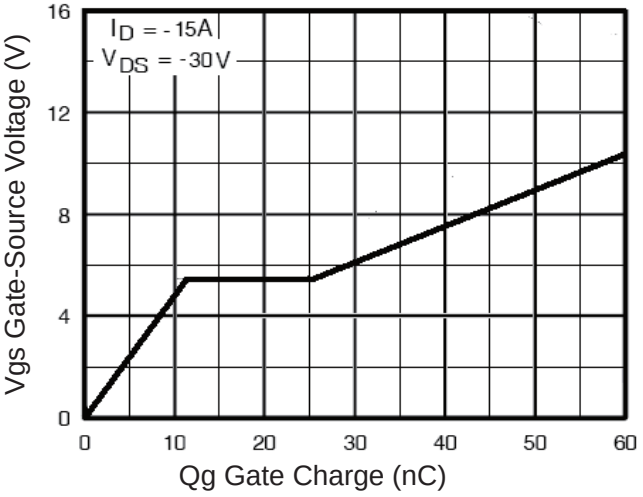


Figure 5 Gate Charge

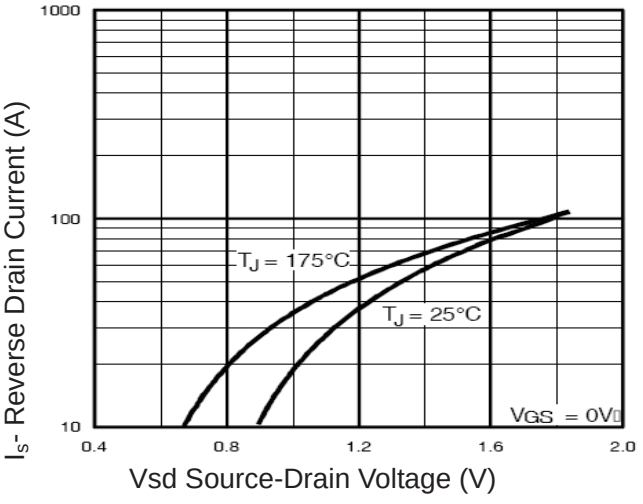


Figure 6 Source- Drain Diode Forward

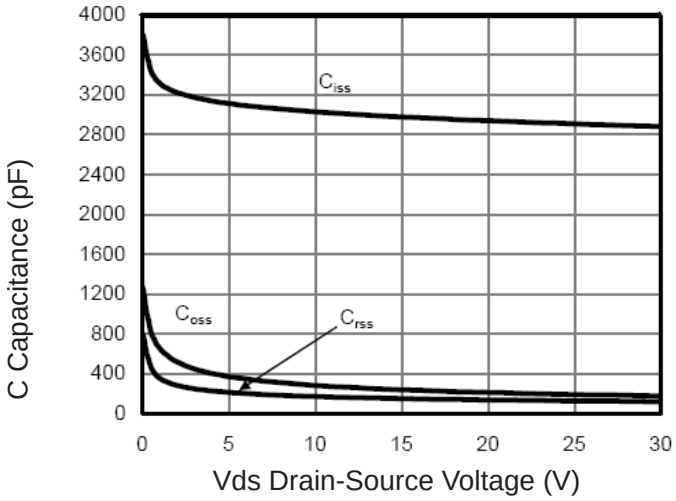


Figure 7 Capacitance vs Vds

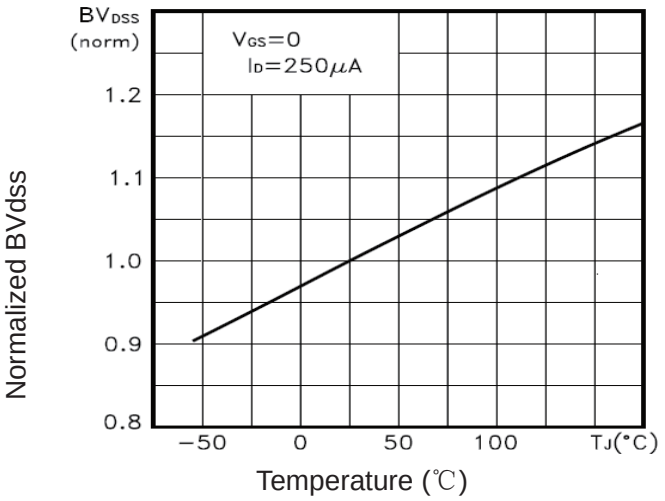


Figure 9 BV_{DSS} vs Junction Temperature

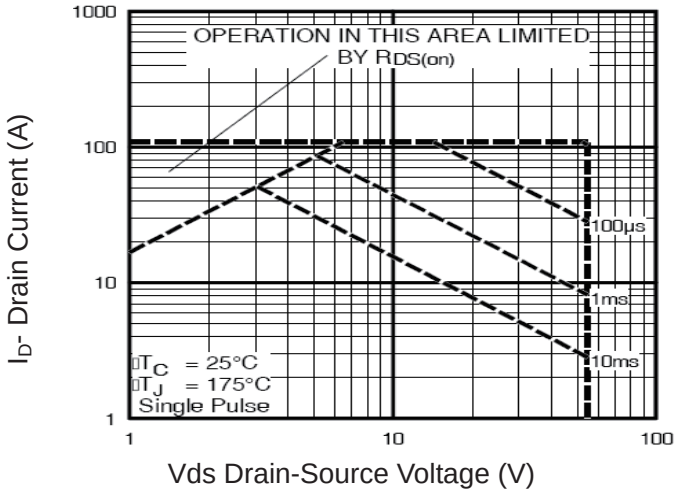


Figure 8 Safe Operation Area

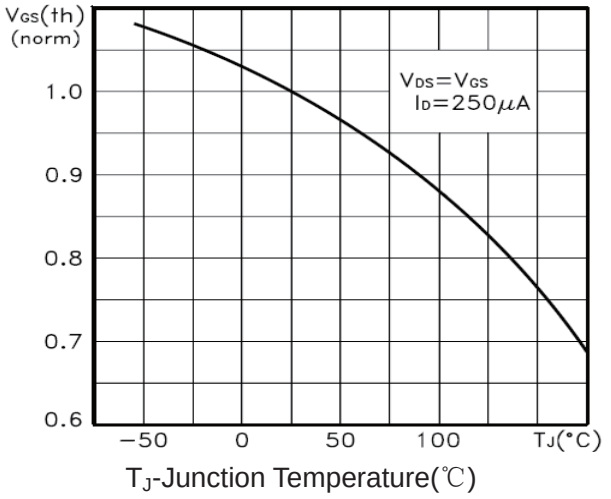


Figure 10 $V_{GS(th)}$ vs Junction Temperature

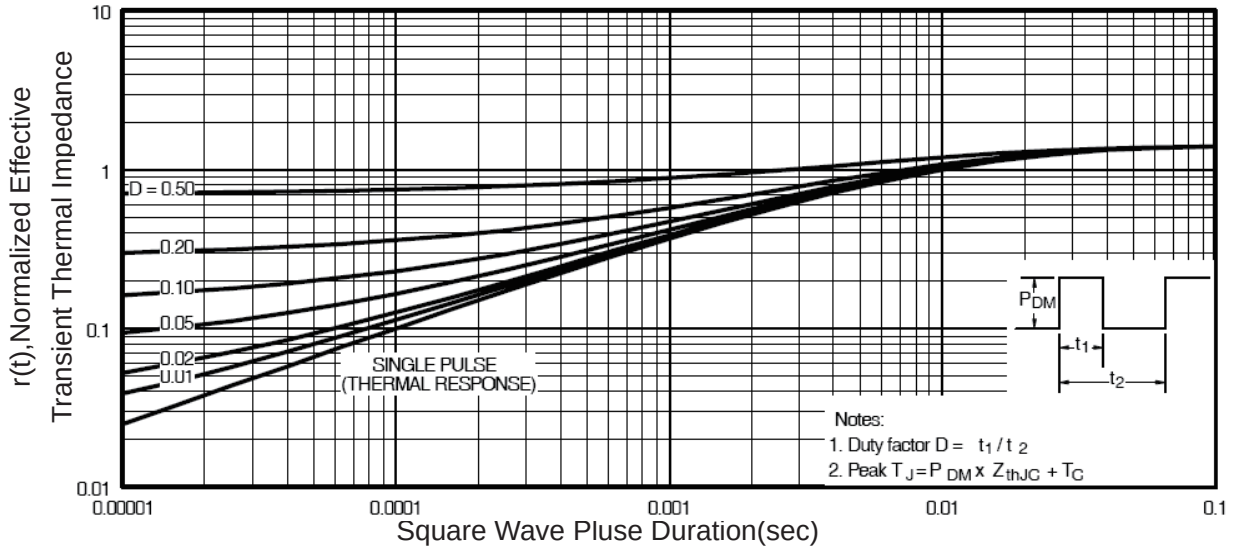


Figure 11 Normalized Maximum Transient Thermal Impedance