

### FTK55P30F P-Channel Power MOSFET

#### DESCRIPTION

The FTK55P30F uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge.

This device is well suited for high current load applications.

- High density cell design for ultra low  $R_{DS(ON)}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
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#### APPLICATIONS

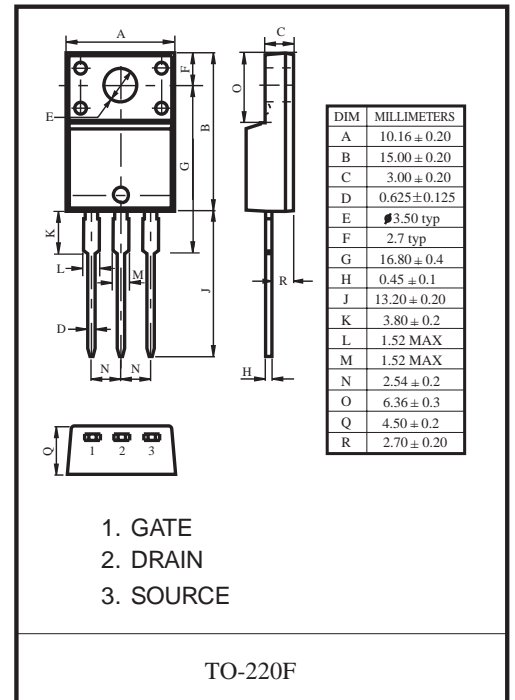
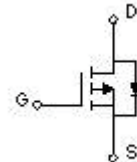
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible Power Supply

#### MARKING



CJPF55P30= Part No.  
XXX=Date Code

#### EQUIVALENT CIRCUIT



#### MAXIMUM RATINGS ( $T_a=25^\circ\text{C}$ unless otherwise noted )

Parameter	Symbol	Limit	Unit
Drain- Source Voltage	$V_{DS}$	- 55	V
Gate- Source Voltage	$V_{GS}$	± 20	V
Continuous Drain Current	$I_D$	- 30	A
Pulsed Drain Current	$I_{DM}$	- 120	A
Single Pulsed Avalanche Energy	$E_{AS}^{(1)}$	225	mJ
Power Dissipation	$P_D$	2	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	- 55~+150	$^\circ\text{C}$
Lead Temperature for Soldering Purposes(1/8" from case for 10s)	$L \ T$	260	$^\circ\text{C}$

(1). $E_{AS}$  condition:  $V_{DS}=- 5V, L=0.5mH, R_G=25\Omega$ , Starting  $T_J = 25^\circ\text{C}$



# FTK55P30F

## Electrical characteristics (T<sub>a</sub>=25°C unless otherwise noted)

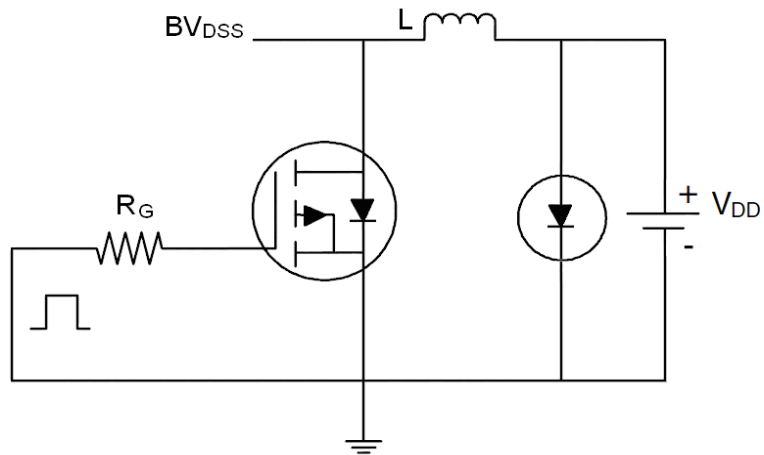
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Off characteristics</b>						
Drain - source breakdown voltage	V <sub>(BR) DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-55			V
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = -55V, V <sub>GS</sub> =0V			-1	μA
Gate - body leakage current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			±100	nA
<b>On characteristics (note1)</b>						
Gate - threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = -250μA	-2.0		-4	V
Static drain - source on - state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -15A			40	mΩ
Forward transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -25V, I <sub>D</sub> = -16A	8			S
<b>Dynamic characteristics (note 2)</b>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -30V, V <sub>GS</sub> =0V, f =1MHz		3500		pF
Output capacitance	C <sub>oss</sub>			240		
Reverse transfer capacitance	C <sub>rss</sub>			153		
<b>Switching characteristics (note 2)</b>						
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = -30V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -15A		56		nC
Gate - source charge	Q <sub>GS</sub>			11		
Gate - drain charge	Q <sub>gd</sub>			24		
Turn - on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = -30V, I <sub>D</sub> = -15A V <sub>GS</sub> = -10V, R <sub>G</sub> = 3Ω,		12		ns
Turn - on rise time	t <sub>r</sub>			15		
Turn - off delay time	t <sub>d(off)</sub>			38		
Turn - off fall time	t <sub>f</sub>			15		
<b>Drain-Source Diode Characteristics</b>						
Drain - source diode forward voltage(note1)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> = -24A			-1.2	V
Continuous drain - source diode forward current (note3)	I <sub>S</sub>				-30	A
Pulsed drain - source diode forward current	I <sub>SM</sub>				-120	A

Notes:

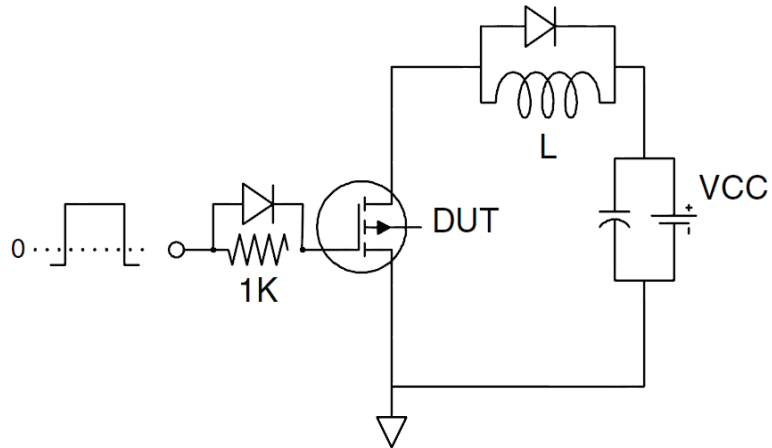
1. Pulse Test : Pulse Width ≤ 300μs, duty cycle ≤ 2%.
2. Guaranteed by design, not subject to production.

## Test Circuit

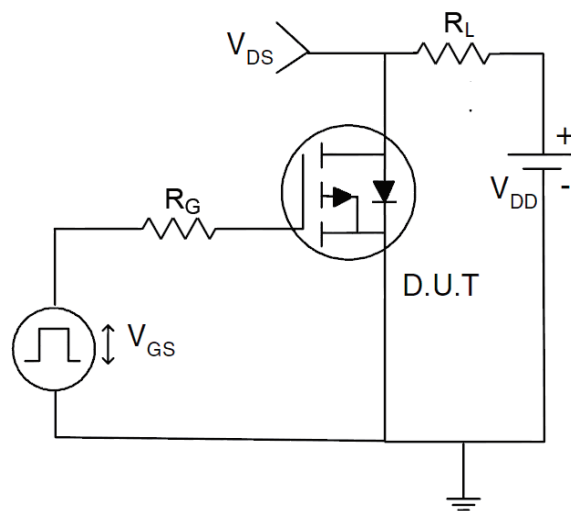
### 1) E<sub>AS</sub> Test Circuit



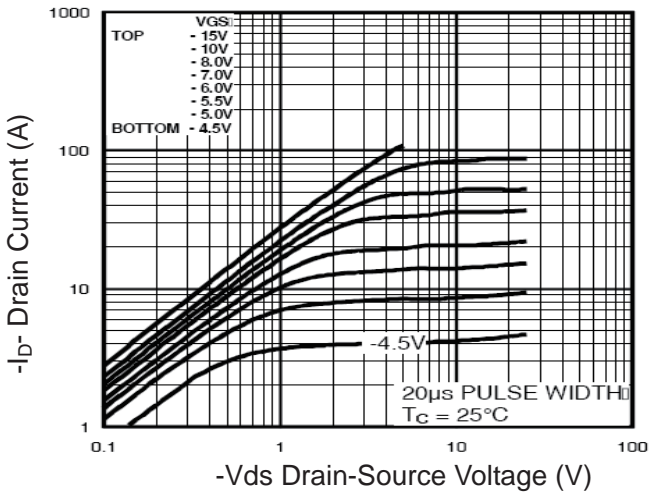
### 2) Gate Charge Test Circuit



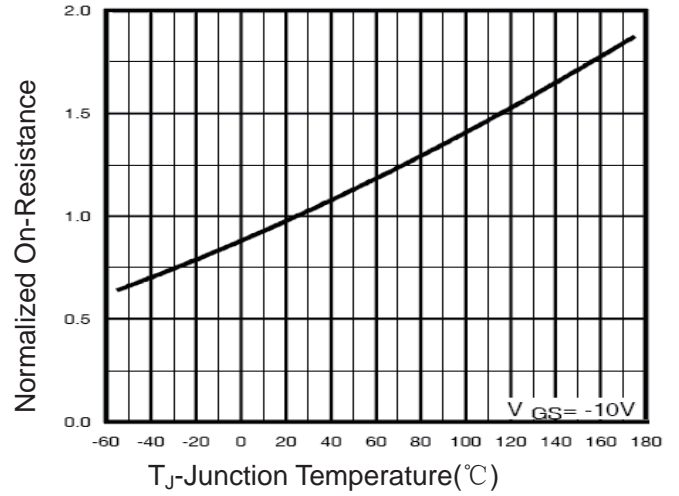
### 3) Switch Time Test Circuit



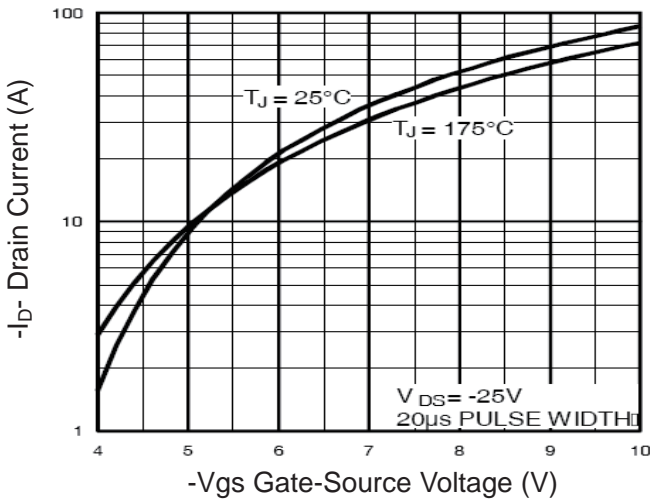
## Typical Electrical and Thermal Characteristics (curves)



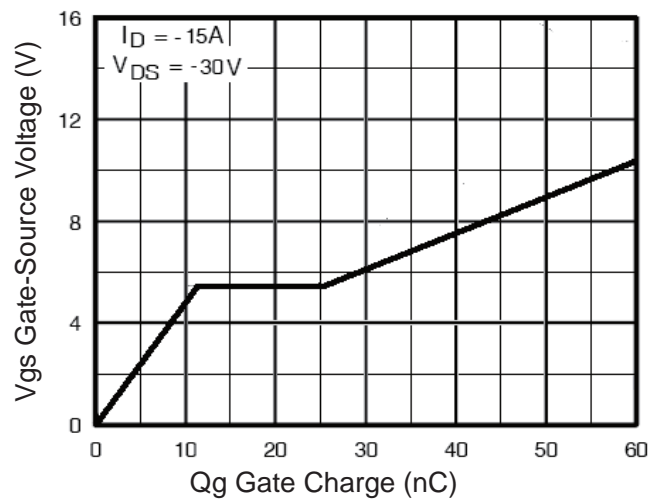
**Figure 1 Output Characteristics**



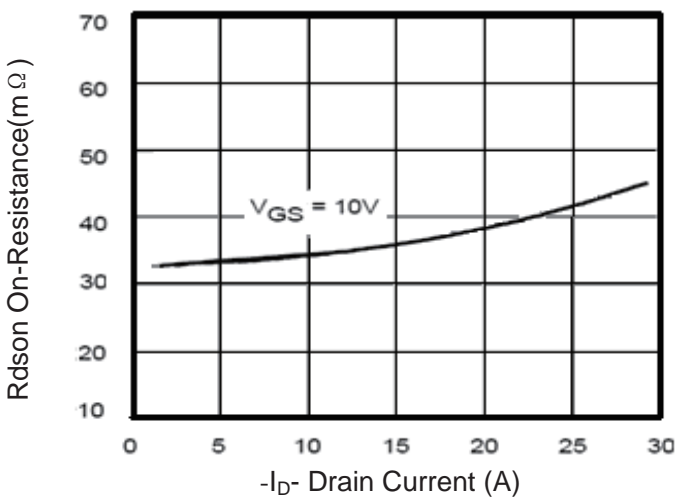
**Figure 4 Rdson-Junction Temperature**



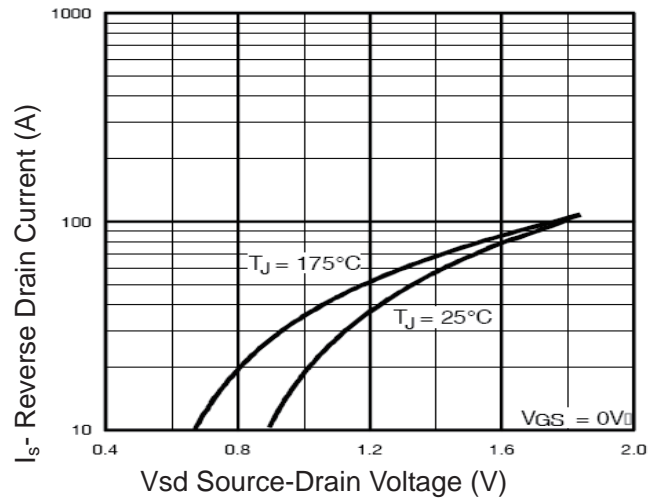
**Figure 2 Transfer Characteristics**



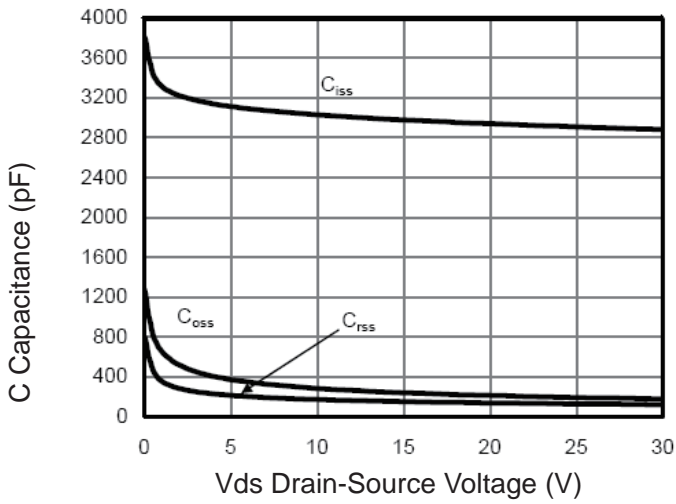
**Figure 5 Gate Charge**



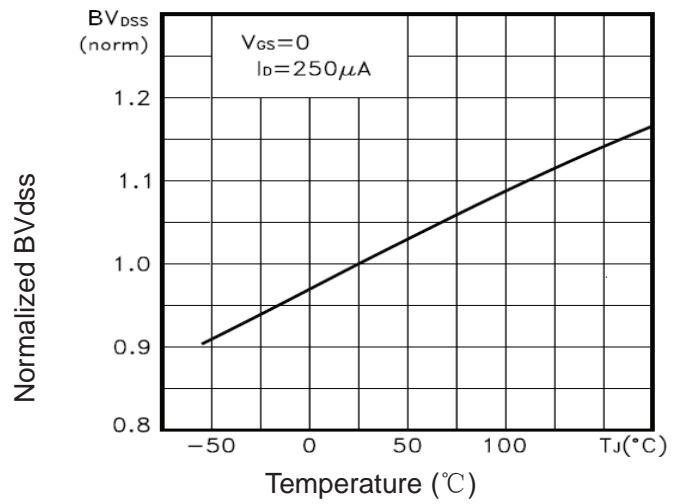
**Figure 3 Rdson- Drain Current**



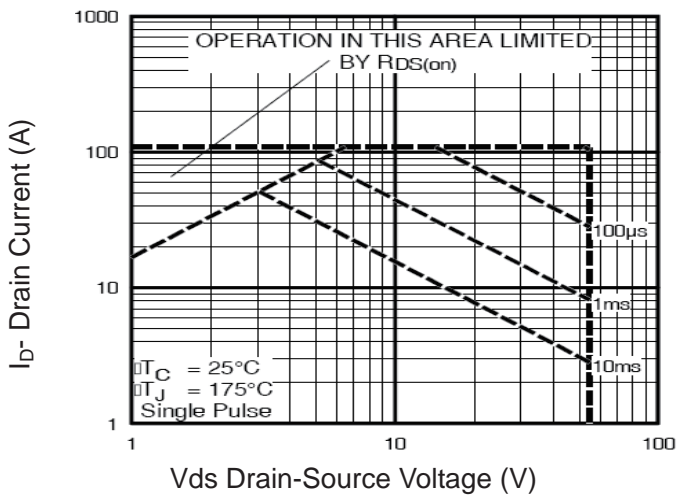
**Figure 6 Source- Drain Diode Forward**



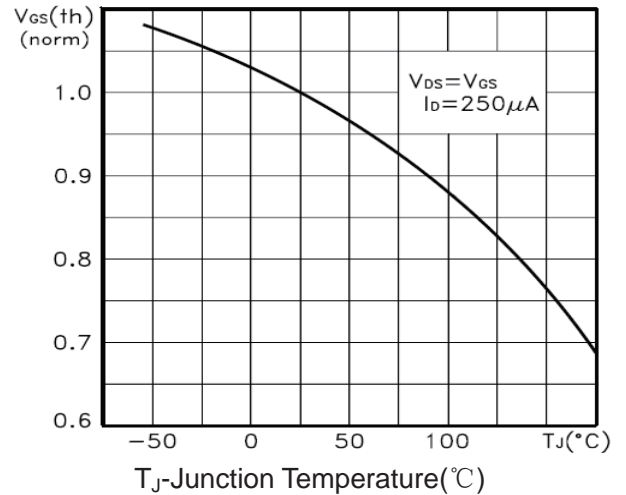
**Figure 7 Capacitance vs Vds**



**Figure 9 BV<sub>DSS</sub> vs Junction Temperature**



**Figure 8 Safe Operation Area**



**Figure 10 V<sub>GS(th)</sub> vs Junction Temperature**