

18A, 200V, 0.155Ω , N-CHANNEL POWER MOS FET

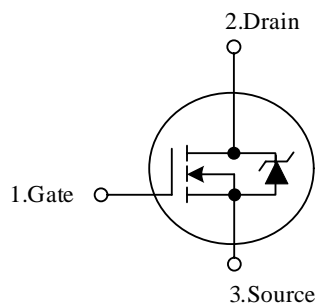
■ DESCRIPTION

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

■ FEATURES

- * 18A, 200V, Low $R_{DS(ON)}$ (0.155Ω)
- * Single Pulse Avalanche Energy Rated
- * Rugged - SOA is Power Dissipation Limited
- * Fast Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance

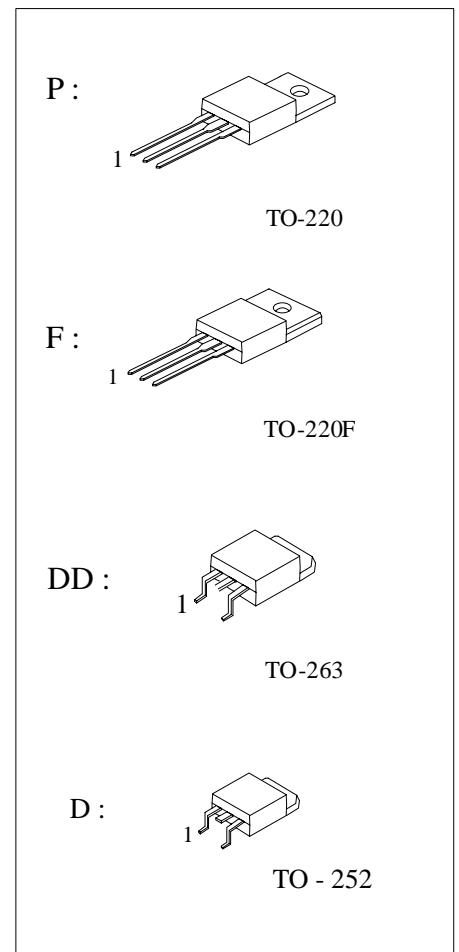
■ SYMBOL



■ ORDERING INFORMATION

Order Number	Package	Pin Assignment			Packing
		1	2	3	
FTK640P	TO-220	G	D	S	Tube
FTK640F	TO-220F	G	D	S	Tube
FTK640DD	TO-263	G	D	S	
FTK640D	TO-252	G	D	S	

Note: Pin Assignment: G: Gate D: Drain S: Source





FTK640D/DD/P/F

■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMET		SYMBOL	RATINGS	UNIT
Drain-Source Voltage (T _J = 25°C ~ 125°C)		V _{DS}	200	V
Drain to Gate Voltage (R _{GS} = 20kΩ, T _J = 25°C ~ 125°C)		V _{DGR}	200	V
Gate to Source Voltage		I _{GS}	±20	V
Drain Current	Continuous	I _D	18	A
	T _A = 100°C	I _D	11	A
	Pulsed	I _{DM}	72	A
Maximum Power Dissipation (T _C = 25°C)		P _D	125 / 40	W
Derating factor (FTK640P / FTK640F)			1.0 / 0.32	W/°C
Single Pulse Avalanche Energy Rating (V _{DD} = 50V, starting T _J = 25°C, L = 3.3mH, R _G = 25Ω, I _{AS} = 19.4A)		E _{AS}	580	mJ
Operating Temperature Range		T _J	-40 ~ +150	°C
Storage Temperature Range		T _{STG}	-40 ~ +150	°C

Note: 1. Signified recommend operating range that indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits.

2. Absolute maximum ratings indicate limits beyond which damage to the device may occur.

■ ELECTRICAL SPECIFICATIONS (T_C = 25°C, unless Otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 16)	200			V
Gate to Threshold Voltage	V _{GS(THR)}	V _{GS} = V _{DS} , I _D = 250μA	2.0		4.0	V
On-State Drain Current (Note 1)	I _{D(ON)}	V _{DS} > I _{D(ON)} × R _{DS(ON)MAX} , V _{GS} = 10V	18			A
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} = 0V			1	μA
		V _{DS} = 0.8 × Rated BV _{DSS} , V _{GS} = 0V, T _J = 125°C			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V			±100	nA
Drain to Source On Resistance (Note 1)	R _{DS(ON)}	I _D = 9.0A, V _{GS} = 10V		0.125	0.15	Ω
Forward Transconductance (Note 1)	g _{FS}	V _{DS} > 10V I _D = 11A	6.7	10		S
Turn-On Delay Time	t _{DLY(ON)}	V _{DD} = 100V, I _D ≈ 19.4A, R _{GS} = 25Ω,		20	50	ns
Rise Time	t _R			190	390	ns
Turn-Off Delay Time	t _{DLY(OFF)}			55	120	ns
Fall Time	t _F			80	170	ns
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10V, I _D = 19.4A, V _{DS} = 0.8 × Rated BV _{DSS}		31	40	nC
Gate to Source Charge	Q _{GS}			8.6		nC
Gate to Drain "Miller" Charge	Q _{GD}			13.5		nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz		1220	1600	pF
Output Capacitance	C _{OSS}			220	290	pF
Reverse - Transfer Capacitance	C _{RSS}			30	40	pF

Note: 1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

2. MOSFET Switching Times are Essentially Independent of Operating Temperature.

3. Gate Charge is Essentially Independent of Operating Temperature.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction-Ambient (FTK640P)	θ_{JA}	62	°C / W
Thermal Resistance Junction-Case (FTK640P)	θ_{JC}	1.0	

■ SOURCE TO DRAIN DIODE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Source to Drain Diode Voltage (Note 1)	V_{SD}	$I_{SD} = 11A, V_{GS} = 0V$			1.3	V
Continuous Source to Drain Current	I_{SD}	Note 2			18	A
Pulse Source to Drain Current	I_{SDM}	Note 2			72	A
Reverse Recovery Time	t_{RR}	$I_{SD} = 19.4A,$ $di_{SD}/dt = 100 A/\mu s$		140		ns
Reverse Recovery Charge	Q_{RR}			0.69		μC

Note:

1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Modified MOSFET symbol showing the integral reverse P-N junction diode as below.

Typical Performance Curves Unless Otherwise Specified

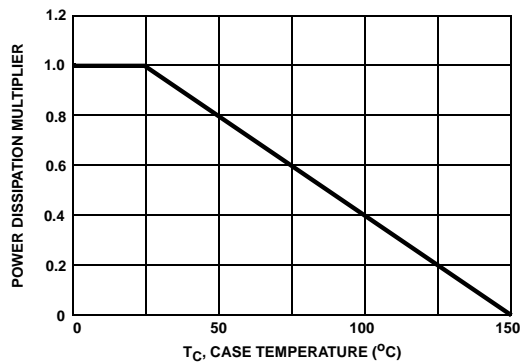


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

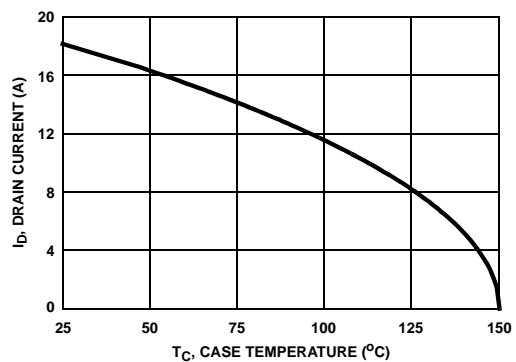


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

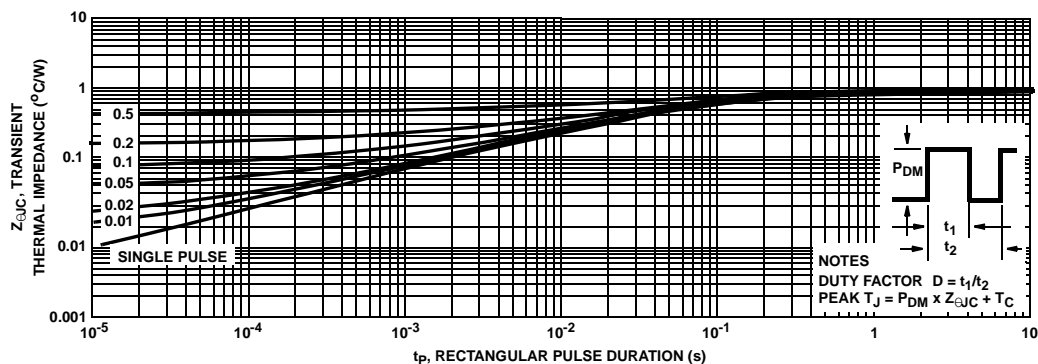


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

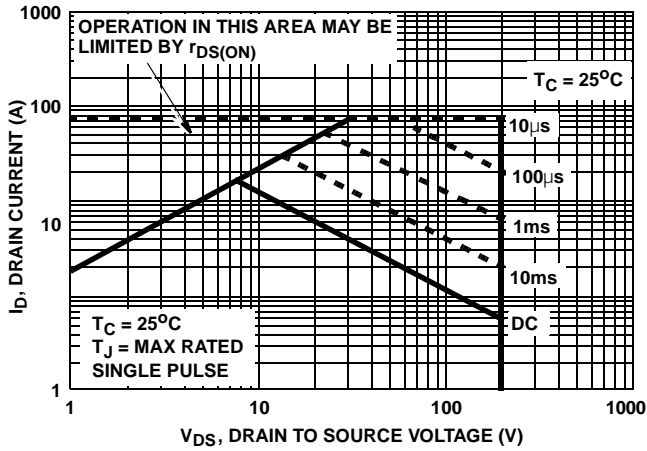


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

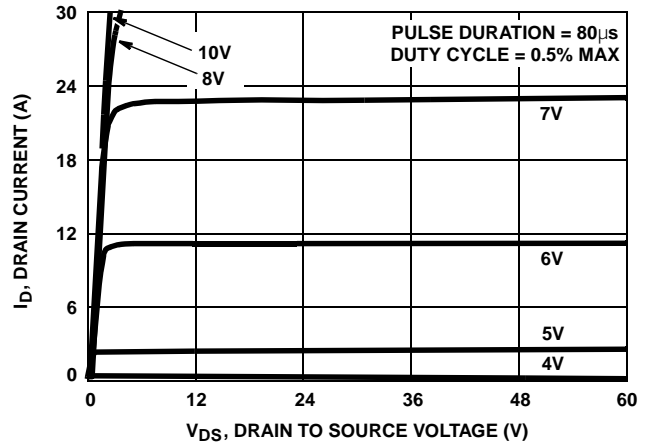


FIGURE 5. OUTPUT CHARACTERISTICS

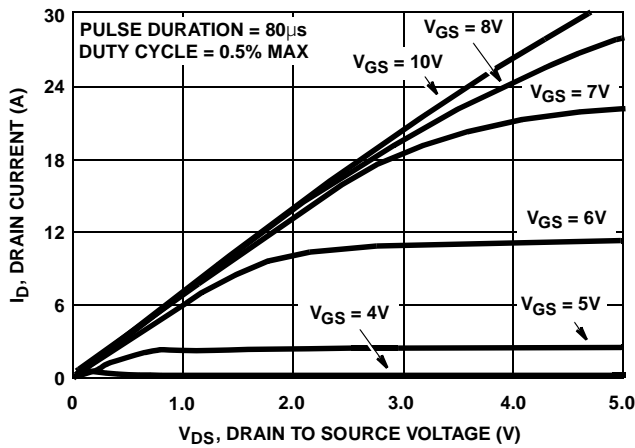


FIGURE 6. SATURATION CHARACTERISTICS

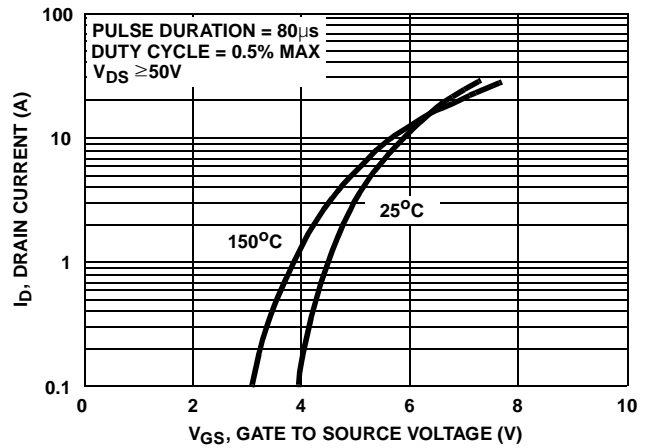


FIGURE 7. TRANSFER CHARACTERISTICS

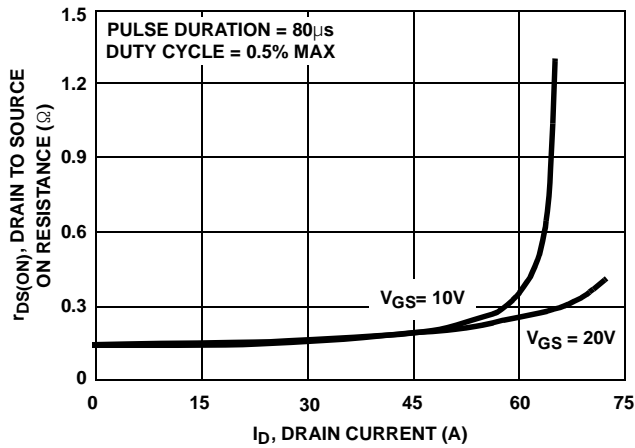


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

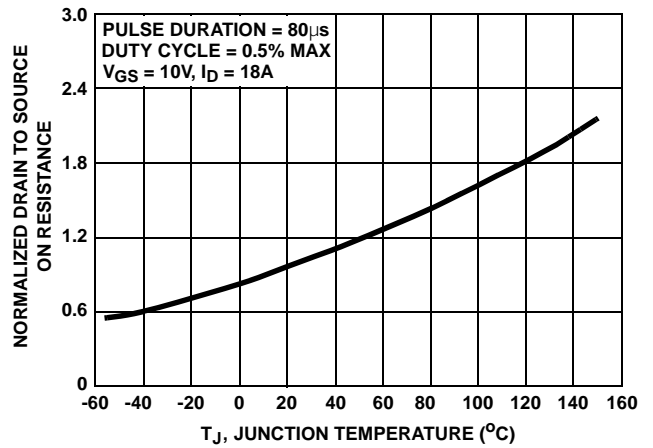


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

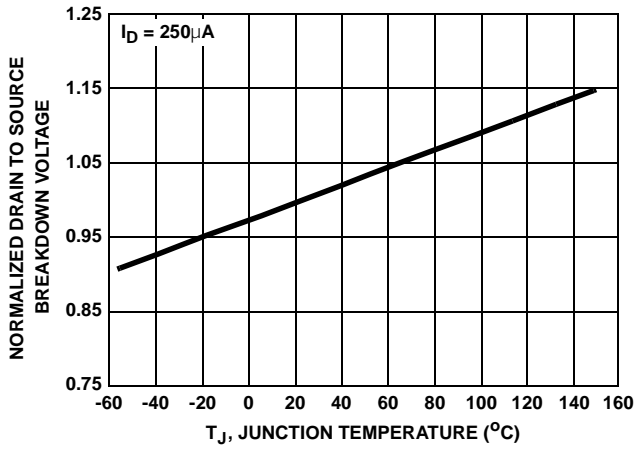


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

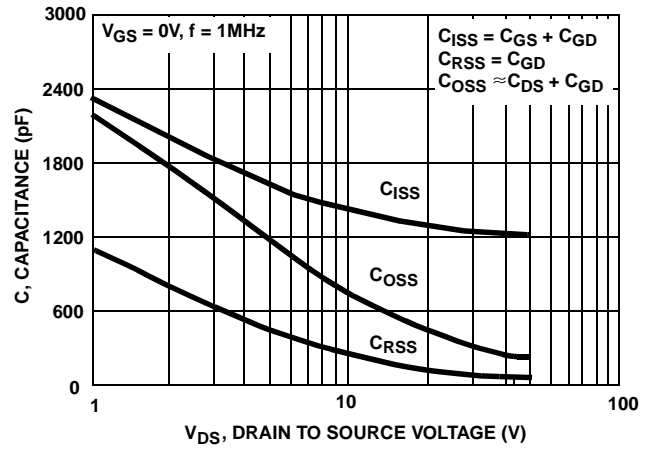


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

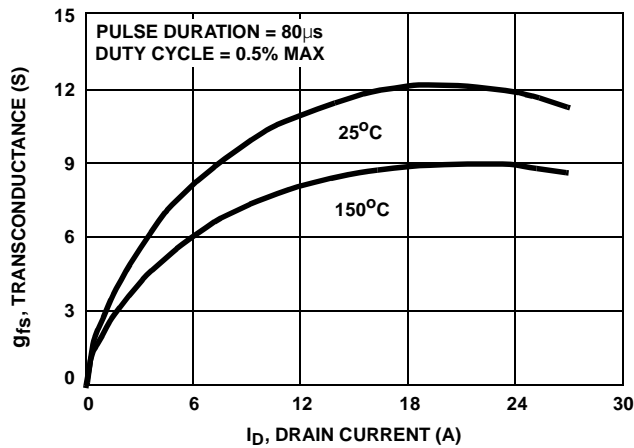


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

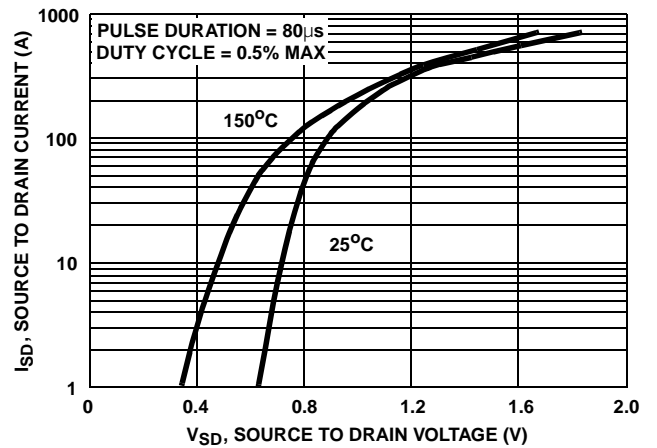


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

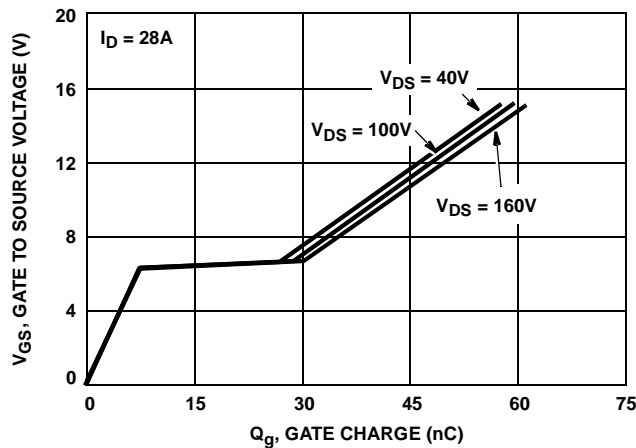


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

■ TEST CIRCUITS AND WAVEFORMS

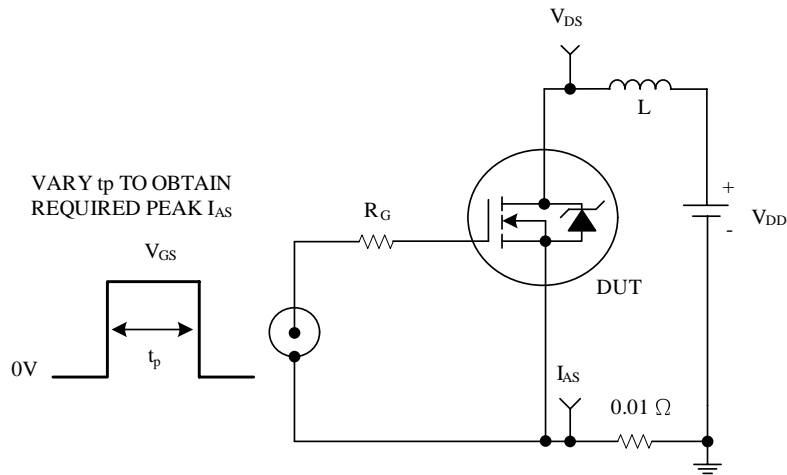


FIGURE 1. UNCLAMPED ENERGY TEST CIRCUIT

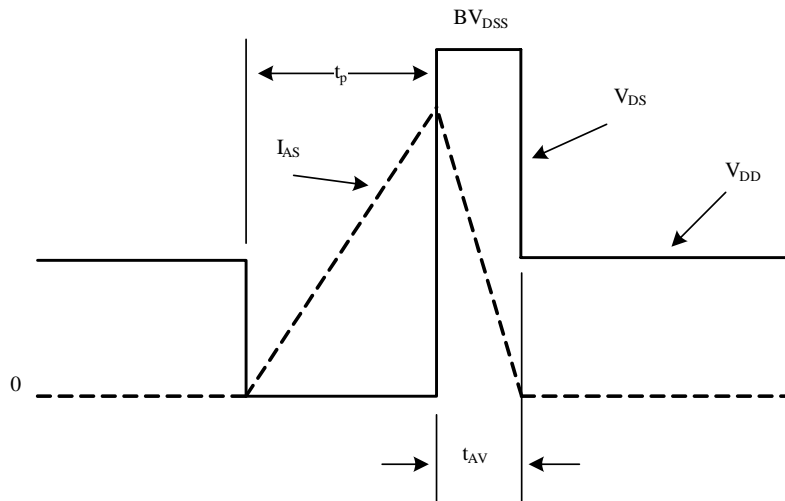


FIGURE 2. UNCLAMPED ENERGY WAVEFORMS

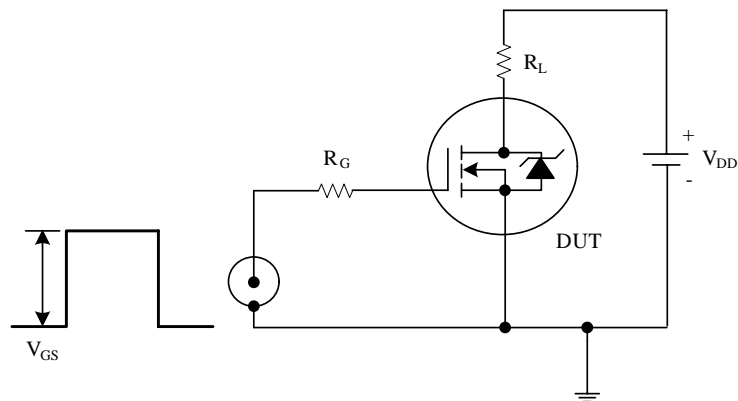


FIGURE 3. SWITCHING TIME TEST CIRCUIT

■ TEST CIRCUITS AND WAVEFORMS(cont.)

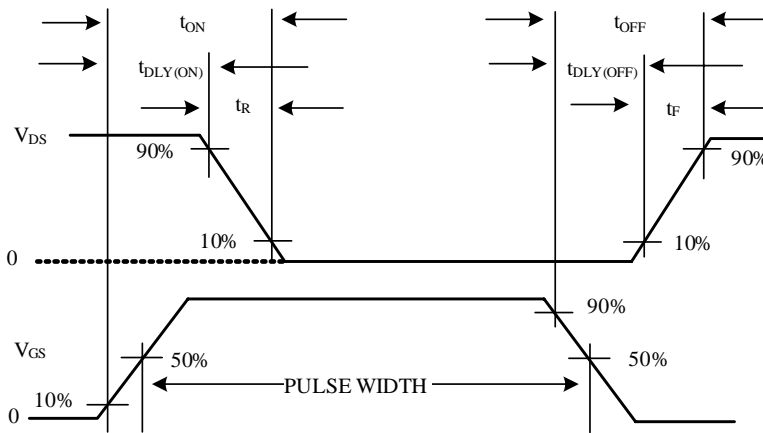


FIGURE 4. RESISTIVE SWITCHING WAVEFORMS

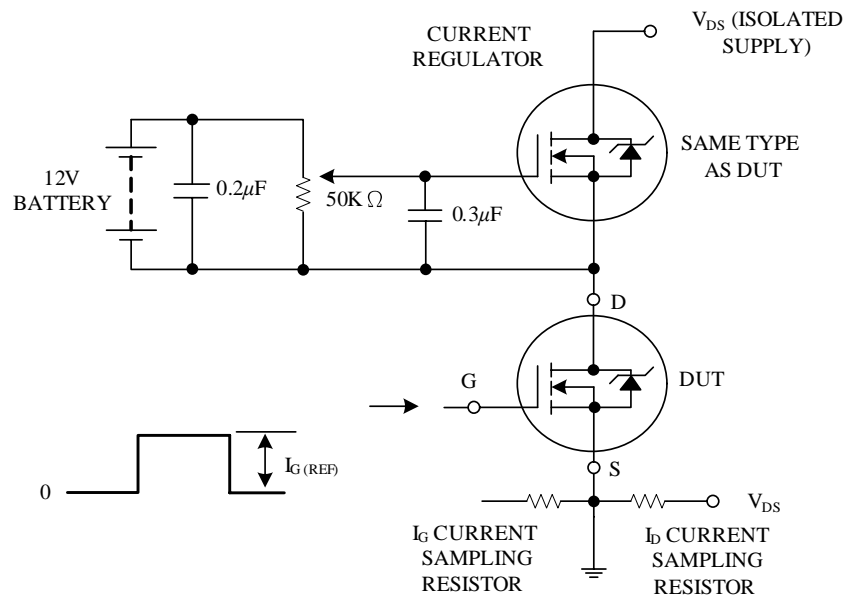


FIGURE 5. GATE CHARGE TEST CIRCUIT

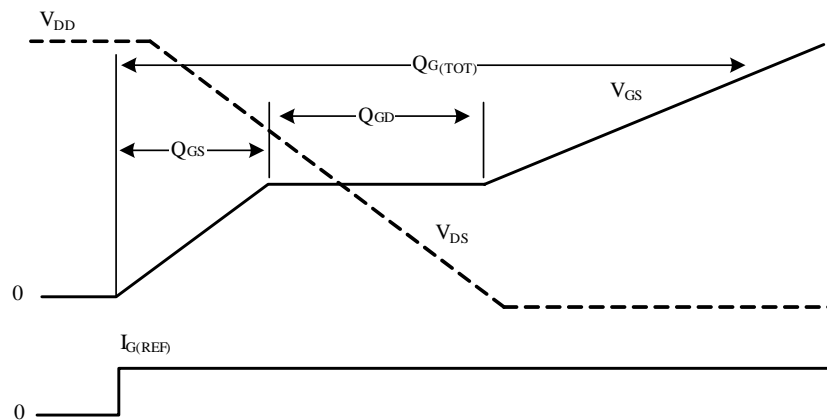


FIGURE 6. GATE CHARGE WAVEFORMS