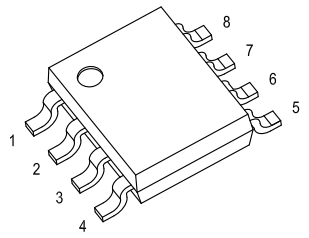
N Channel +P Channel MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$MAX	I_D
60V	58mΩ@10V	4.5A
	72mΩ@4.5V	
-60V	80mΩ@-10V	-3.5A
	100mΩ@-4.5V	

SOP8



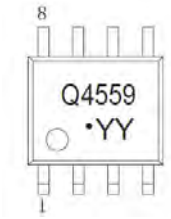
FEATURE

- Surface Mount Package
- Super High Density Cell Design for Extremely Low $R_{DS(ON)}$

APPLICATION

- CCFL Inverter

MARKING



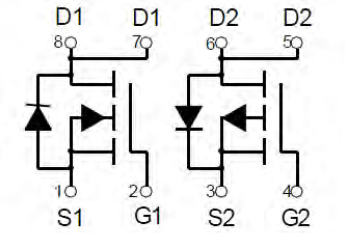
Q4559= Device code

YY=Date Code

Solid dot = Pin1 indicator

Solid dot = Green molding compound device, if none,the normal device.

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
N-MOSFET			
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current (note 1)	I_D	4.5	A
Pulsed Drain Current (tp=10us)	I_{DM}	18	A
Continous Source-Drain Diode Current	I_S	4.5	A
P-MOSFET			
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current (note 1)	I_D	-3.5	A
Pulsed Drain Current (tp=10us)	I_{DM}	-14	A
Continous Source-Drain Diode Current	I_S	-3.5	A
Temperature and Thermal Resistance			
Power Dissipation	P_D	2	W
Thermal Resistance from Junction to Ambient (note 1)	$R_{\theta JA}$	62.5	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~+150	℃
Lead Temperature for Soldering Purposes(1/8'' from case for 10 s)	T_L	260	℃

N-ch MOSFET ELECTRICAL CHARACTERISTICS(T_a=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC CHARACTERISTICS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	60			V
Zero gate voltage drain current	I_{DSS}	V_{DS} = 60V,V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V			±100	nA
Gate threshold voltage (note 2)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	1	2.1	3	V
Drain-source on-resistance(note 2)	$R_{DS(on)}$	V_{GS} =10V, I_D =4.3A		40	58	mΩ
		V_{GS} =4.5V, I_D =3.9A		55	72	mΩ
Forward tranconductance(note 2)	g_{FS}	V_{DS} =15V, I_D =4.3A		15		S
Diode forward voltage	V_{SD}	I_S=1.7A, V_{GS} = 0V			1.2	V
DYNAMIC CHARACTERISTICS (note 4)						
Input Capacitance	C_{iss}	V_{DS} =15V,V_{GS} =0V,f =1MHz		665		pF
Output Capacitance	C_{oss}			75		pF
Reverse Transfer Capacitance	C_{rss}			40		pF
Gate Resistance	R_g	f=1MHz			3	Ω
SWITCHING CHARACTERISTICS (note 3,4)						
Turn-on delay time	$t_{d(on)}$	V_{GEN}=4.5V,V_{DD}=30V, I_D=3.4A, R_G=1Ω， R_L=8.8Ω			25	ns
Turn-on rise time	t_r				100	ns
Turn-off delay time	$t_{d(off)}$				25	ns
Turn-off fall time	t_f				15	ns
Total Gate Charge	Q_g	V_{DS}=30V,I_D=4.3A, V_{GS}=4.5V			9	nC
Gate-Source Charge	Q_{gs}			2.3		nC
Gate-Drain Charge	Q_{gd}			2.6		nC

P-ch MOSFET ELECTRICAL CHARACTERISTICS(T_a=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC CHARACTERISTICS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-60			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-60V,V_{GS} = 0V			-1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V			±100	nA
Gate threshold voltage (note 2)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-1	-2.8	-3	V
Drain-source on-resistance(note 2)	$R_{DS(on)}$	V_{GS} =-10V, I_D =-3.1A		60	80	mΩ
		V_{GS} =-4.5V, I_D =-0.2A		92	100	mΩ
Forward tranconductance(note 2)	g_{FS}	V_{DS} =-15V, I_D =-3.1A		8.5		S
Diode forward voltage	V_{SD}	I_S=-2A, V_{GS} = 0V			-1.2	V
DYNAMIC CHARACTERISTICS (note 4)						
Input Capacitance	C_{iss}	V_{DS} =-15V,V_{GS} =0V,f =1MHz		650		pF
Output Capacitance	C_{oss}			95		pF
Reverse Transfer Capacitance	C_{rss}			60		pF
Gate Resistance	R_g	f=1MHz			20	Ω
SWITCHING CHARACTERISTICS (note 3,4)						
Turn-on delay time	$t_{d(on)}$	V_{GEN}=-4.5V,V_{DD}=-30V, I_D=-2.4A,R_G=1Ω ， R_L=12.5Ω			45	ns
Turn-on rise time	t_r				105	ns
Turn-off delay time	$t_{d(off)}$				60	ns
Turn-off fall time	t_f				45	ns
Total Gate Charge	Q_g	V_{DS}=-30V,I_D=-3.1A, V_{GS}=-4.5V			12	nC
Gate-Source Charge	Q_{gs}			2.2		nC
Gate-Drain Charge	Q_{gd}			3.7		nC

Notes :

1.Surface mounted on FR4 board using the minimum recommended pad size.

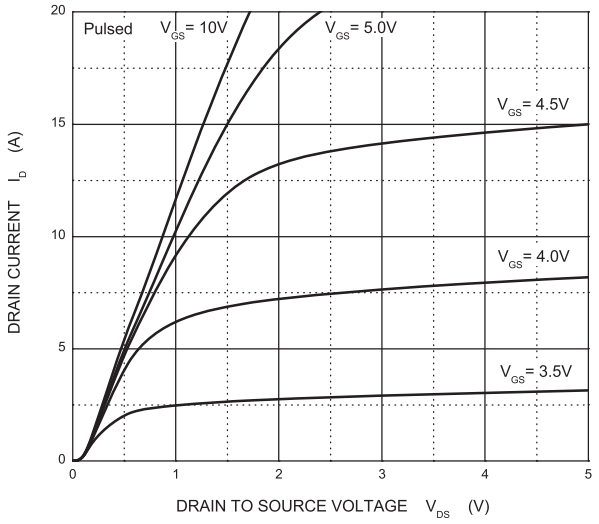
2. Pulse Test : Pulse width=300μs, duty cycle≤2%.

3. Switching characteristics are independent of operating junction temperature.

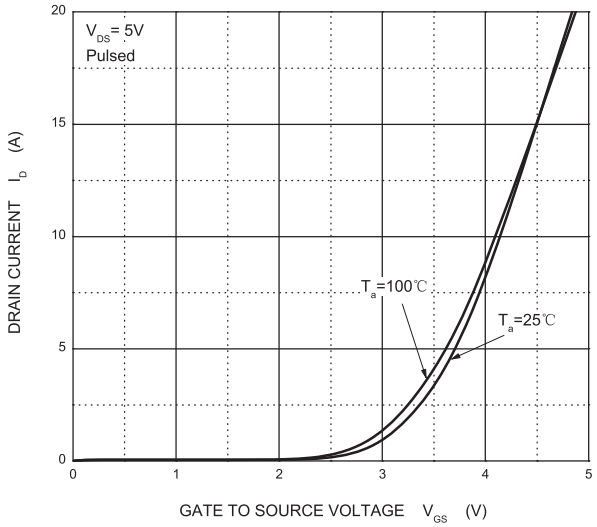
4. Graranted by design， not subject to producting.

N-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

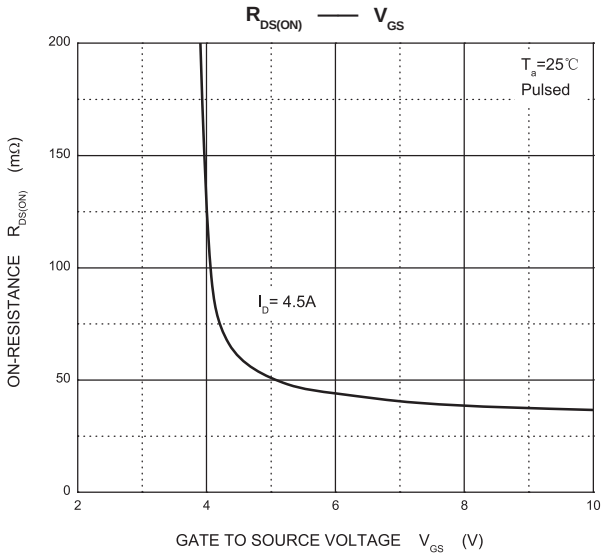
Output Characteristics



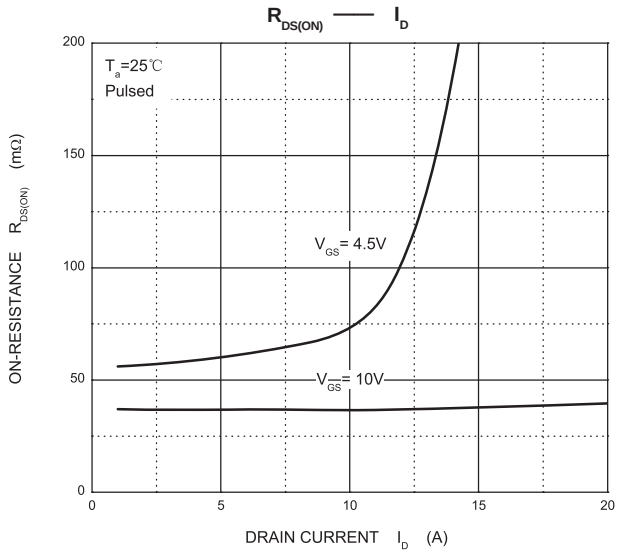
Transfer Characteristics



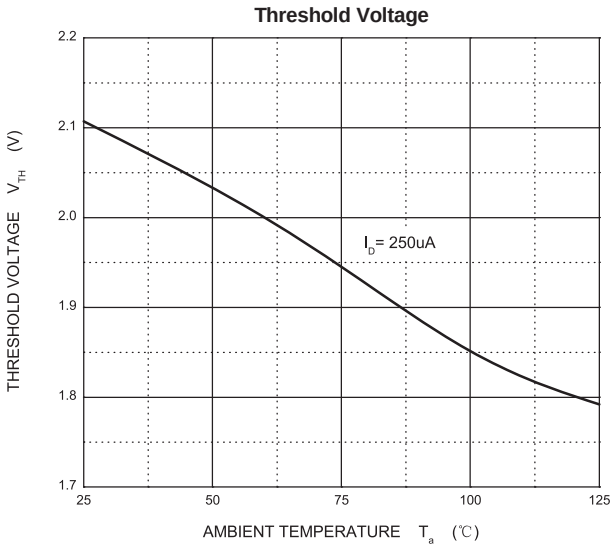
$R_{DS(ON)}$ — V_{GS}



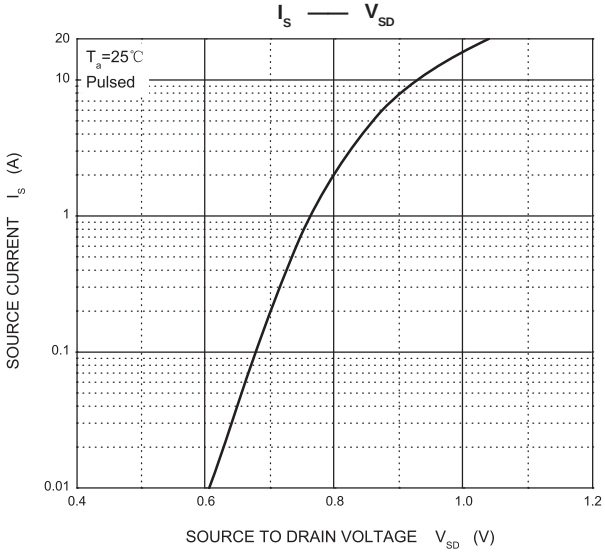
$R_{DS(ON)}$ — I_D



Threshold Voltage

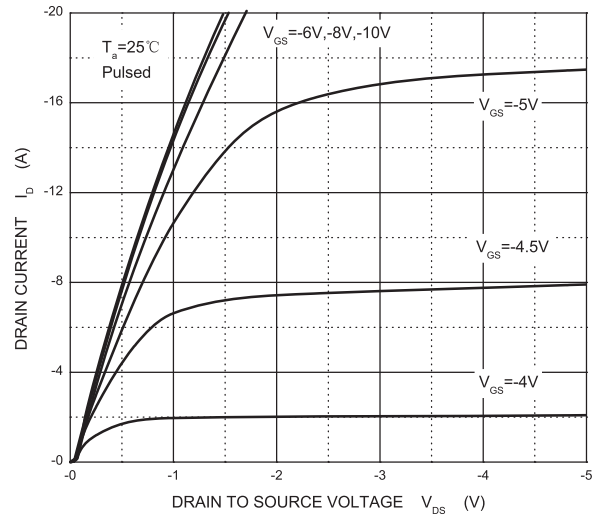


I_S — V_{SD}

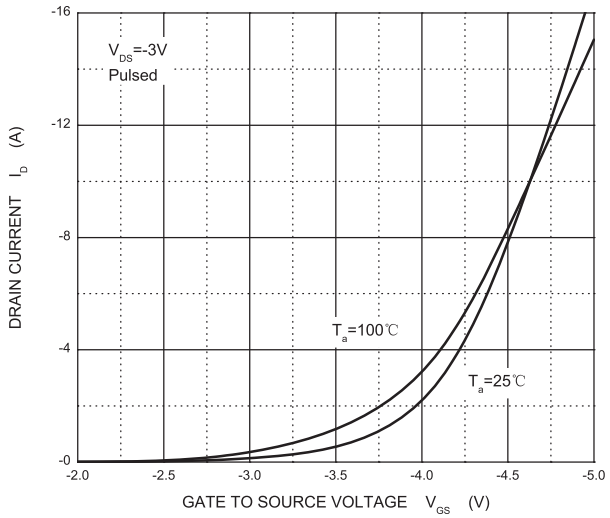


P-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

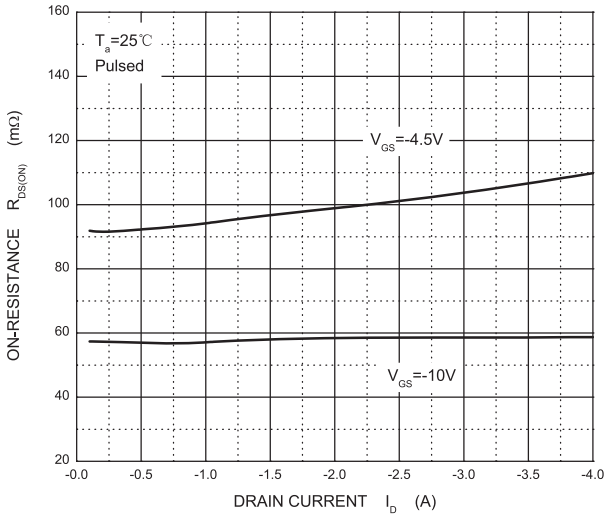
Output Characteristics



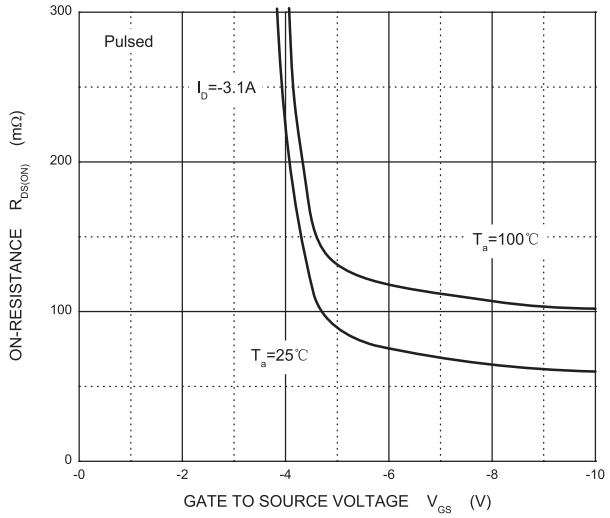
Transfer Characteristics



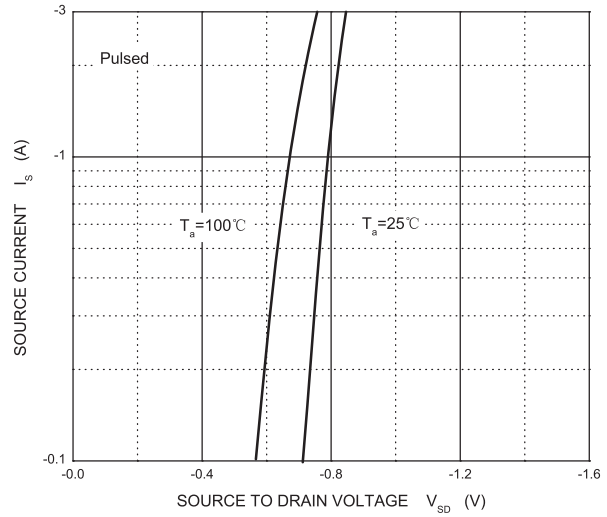
$R_{DS(ON)}$ —— I_D



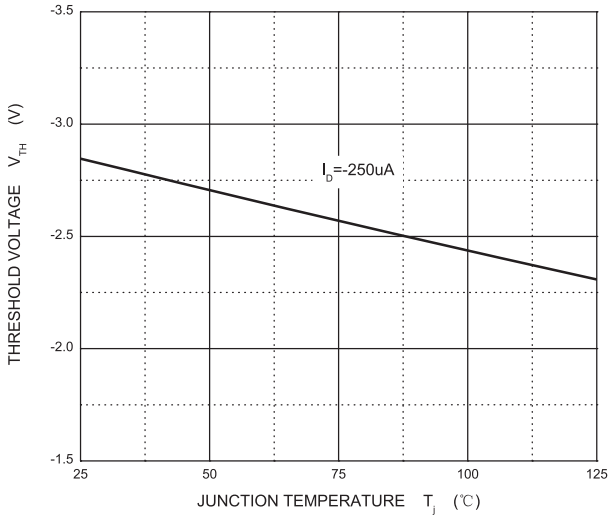
$R_{DS(ON)}$ —— V_{GS}



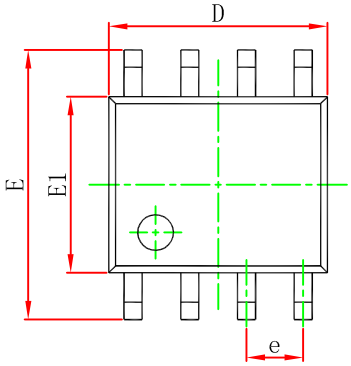
I_S —— V_{SD}

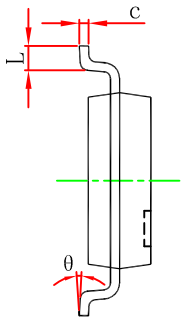


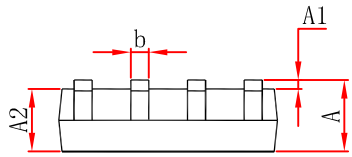
Threshold Voltage



SOP8 Package Outline Dimensions

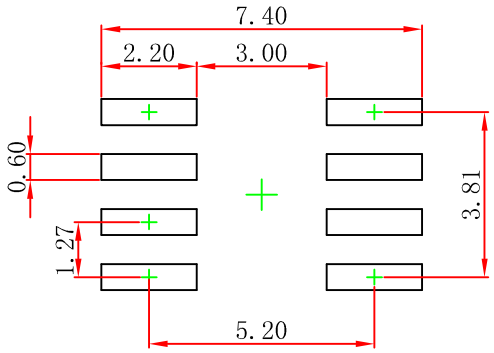






Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270（BSC）		0.050（BSC）	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOP8 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.