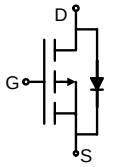
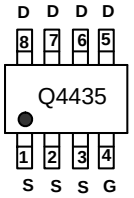
FTK4435

DESCRIPTION

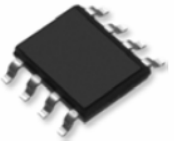
The FTK4435 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge .It has been optimized for power management applications requiring a wide range of gave drive voltage ratings (4.5V – 25V).



Schematic diagram



Marking and pin Assignment



SOP-8 top view

GENERAL FEATURES

- V_{DS} = -30V,I_D = -9.1A
  $R_{DS(ON)}$ < 35mΩ @ V_{GS}=-4.5V
  $R_{DS(ON)}$ < 24mΩ @ V_{GS}=-10V
- High Power and current handing capability
- Lead free product is acquired
- Surface Mount Package

Application

- Battery protection
- Load switch
- Power management

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
Q4435	FTK4435	SOP-8	Ø330mm	12mm	4000 units

ABSOLUTE MAXIMUM RATINGS(TA=25℃unless otherwise noted)

Parameter	Symbol	Value	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	
Continuous Drain Current (t =10s) (note 1)	I_D	-9.1	A
Pulsed Drain Current	I_{DM}	-50	
Drain-Source Diode Forward Current (t =10s) (note 1)	I_S	-2	
Power Dissipation (t =10s)	P_D	1.4	W
Thermal Resistance from Junction to Ambient (t ≤10s) (note 1)	$R_{\theta JA}$	89	℃/W
Junction Temperature	T_J	-55 ~+150	℃
Storage Temperature	T_{stg}	-55 ~+150	

Electrical characteristics (T_a=25℃ unless otherwise noted)

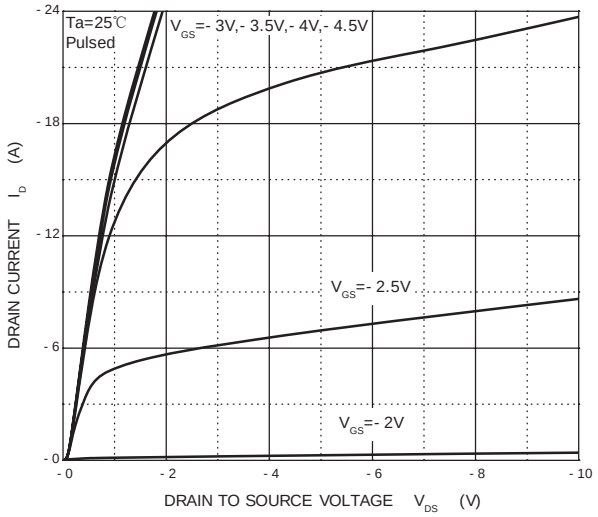
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V, V_{GS}=0V			-1	μA
Gate body Leakage	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-1		-3	V
Drain-Source on-state Resistance (note 2)	$R_{DS(on)}$	V_{GS} =-10V, I_D =-9.1A			24	mΩ
		V_{GS} =-4.5V, I_D =-6.9A			35	
Forward Transconductance (note 2)	g_{Fs}	V_{DS} =-10V, I_D =-9.1A	20			S
Dynamic Characteristics (note 3)						
Input Capacitance	C_{iss}	V_{DS} =-15V,V_{GS} =0V,f =1MHz		1350		pF
Output Capacitance	C_{oss}			215		
Reverse Transfer Capacitance	C_{rss}			185		
Total Gate Charge	Q_g	V_{DS} =-15V,V_{GS} =-10V,I_D =-9.1A			50	nC
		V_{DS} =-15V,V_{GS} =-4.5V,I_D =-9.1A			25	
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			7.5		
Gate Resistance	R_g	f =1MHz		5.8		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=-15V,R_L=15Ω I_D =-1A,V_{GEN}=-10V,R_G=1Ω			15	ns
Rise Time	t_r				15	
Turn-Off Delay Time	$t_{d(off)}$				70	
Fall Time	t_f				25	
Drain-Source Body Diode Characteristics						
Diode Forward Voltage	V_{SD}	I_S=-2A,V_{GS}=0V			-1.2	V

Notes:

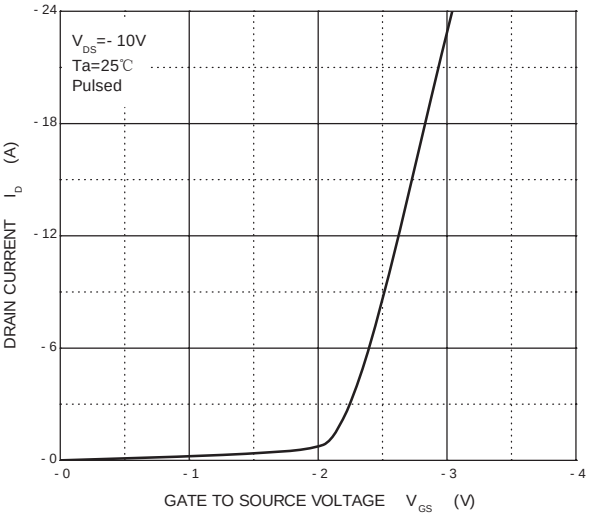
1. Surface mounted on 1”×1” FR4 board.
2. Pulse Test : Pulse Width≤300μs, Duty Cycle ≤2%.
3. Guaranteed by design, not subject to production testing.

Typical Characteristics

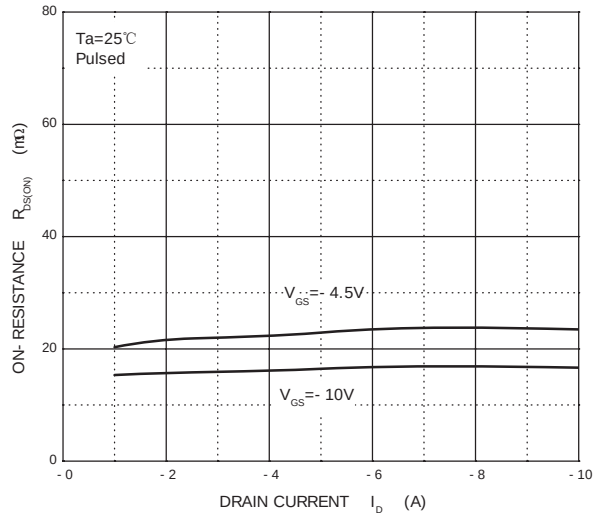
Output Characteristics



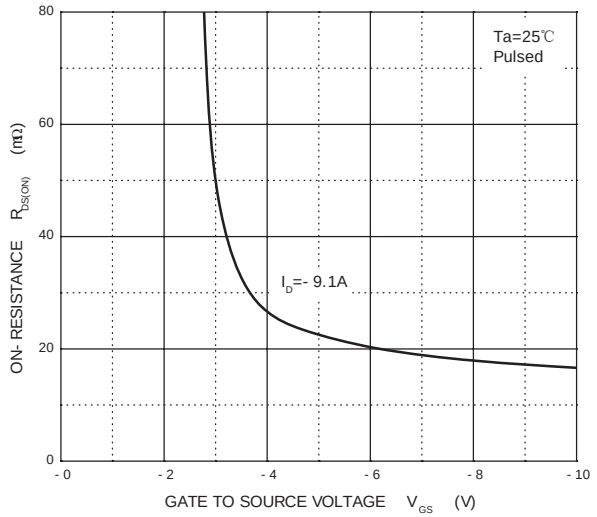
Transfer Characteristics



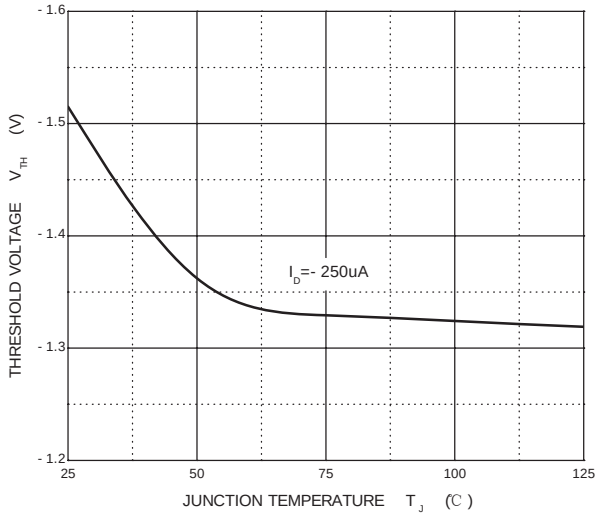
$R_{DS(ON)}$ —— I_D



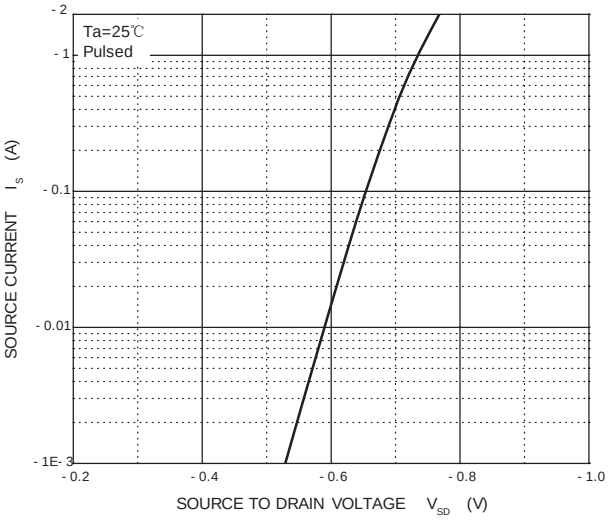
$R_{DS(ON)}$ —— V_{GS}



Threshold Voltage

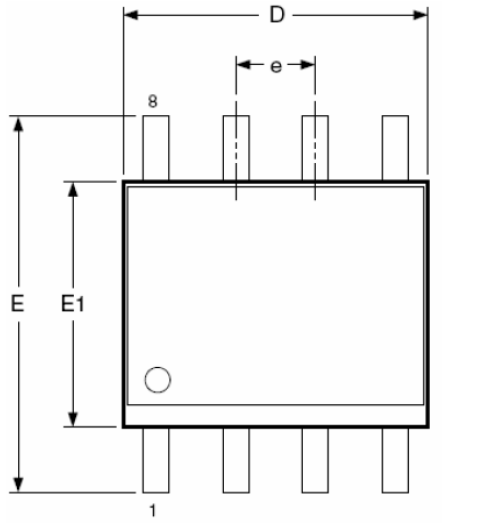


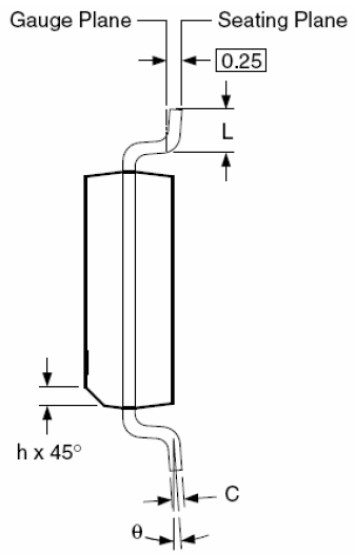
I_S —— V_{SD}

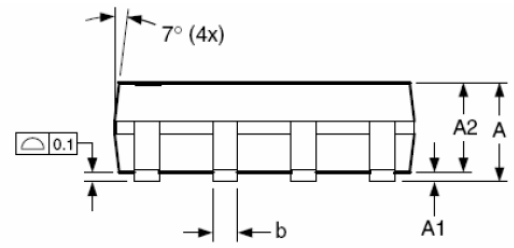


SOP-8 PACKAGE INFORMATION

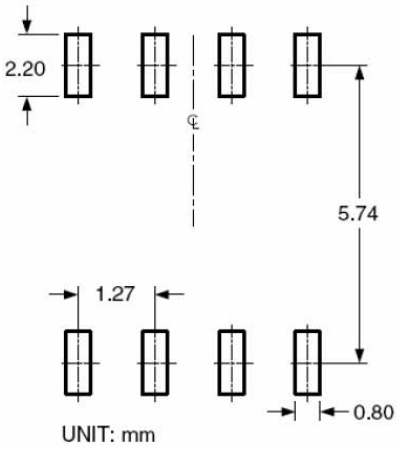
Dimensions in Millimeters (UNIT:mm)







RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
e	1.27 BSC		
E	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

Dimensions in inches

Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E1	0.150	0.154	0.157
e	0.050 BSC		
E	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

NOTES:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.