

## P-Channel Enhancement Mode MOSFET

### Features

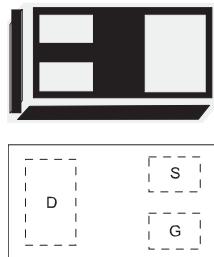
- Lead free product is acquired
- Surface mount package
- P-Channel switch with low  $R_{DS(on)}$
- Operated at low logic level gate drive
- ESD protected gate
- Complementary to FTK2008SOT883

### Application

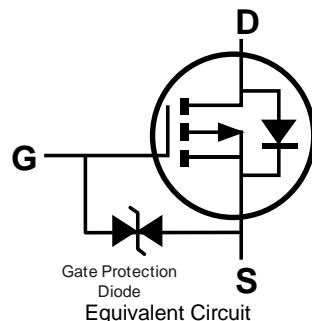
- Load/Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift

### Circuit diagram

### Package and Pin Configuration



DFN1006-3L



### Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-source voltage	$V_{DS}$	-20	V
Typical gate-source voltage	$V_{GS}$	$\pm 12$	V
Continuous drain current (note 1)	$I_D$	-0.66	A
Pulsed drain current ( $t_p=10\mu\text{s}$ )	$I_{DM}$	-1.2	A
Power dissipation (note 2)	$P_D$	100	mW
Thermal resistance from junction to ambient (note 1)	$R_{QJA}$	1250	$^\circ\text{C}/\text{W}$
Junction temperature range	$T_J$	150	$^\circ\text{C}$
Storage temperature range	$T_{STG}$	-55 ~ +150	$^\circ\text{C}$
Lead temperature for soldering purposes (1/8" from case for 10s)	$T_L$	260	$^\circ\text{C}$



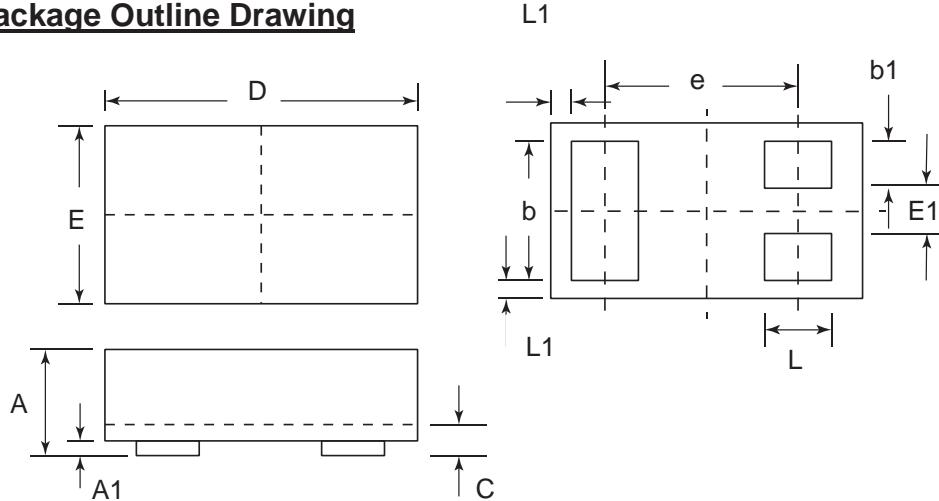
## P-Channel Enhancement Mode MOSFET

**Electrical Characteristics (  $T_A = 25^\circ\text{C}$  unless otherwise noted )**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>STATIC PARAMETERS</b>						
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0\text{V}$ , $I_D = -250\mu\text{A}$	-20			V
Zero gate voltage drain current	$I_{\text{DSS}}$	$V_{DS} = -20\text{V}$ , $V_{GS} = 0\text{V}$			-1	$\mu\text{A}$
Gate-body leakage current	$I_{\text{GSS}}$	$V_{GS} = \pm 10\text{V}$ , $V_{DS} = 0\text{V}$			$\pm 20$	$\mu\text{A}$
Gate threshold voltage (note 2)	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = -250\mu\text{A}$	-0.35		-1.1	V
Drain-source on-resistance (note 2)	$R_{DS(\text{on})}$	$V_{GS} = -4.5\text{V}$ , $I_D = -1\text{A}$			520	$\text{m}\Omega$
		$V_{GS} = -2.5\text{V}$ , $I_D = -0.8\text{A}$			700	
		$V_{GS} = -1.8\text{V}$ , $I_D = -0.5\text{A}$			950	
Forward transconductance (note 2)	$g_{\text{FS}}$	$V_{DS} = -10\text{V}$ , $I_D = -0.54\text{A}$		1.2		S
Diode forward voltage	$V_{SD}$	$I_S = -0.5\text{A}$ , $V_{GS} = 0\text{V}$			-1.2	V
<b>DYNAMIC PARAMETERS (note 4)</b>						
Input capacitance	$C_{\text{iss}}$	$V_{DS} = -16\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$		113	170	$\text{pF}$
Output capacitance	$C_{\text{oss}}$			15	25	
Reverse transfer capacitance	$C_{\text{rss}}$			9	15	
<b>SWITCHING PARAMETERS (note 4)</b>						
Turn-on delay time (note 3)	$t_{d(on)}$	$V_{GS} = -4.5\text{V}$ , $V_{DS} = -10\text{V}$ , $I_D = -200\text{mA}$ , $R_{\text{GEN}} = 10\Omega$		9		ns
Turn-on rise time (note 3)	$t_r$			5.8		
Turn-off delay time (note 3)	$t_{d(off)}$			32.7		
Turn-off fall time (note 3)	$t_f$			20.3		

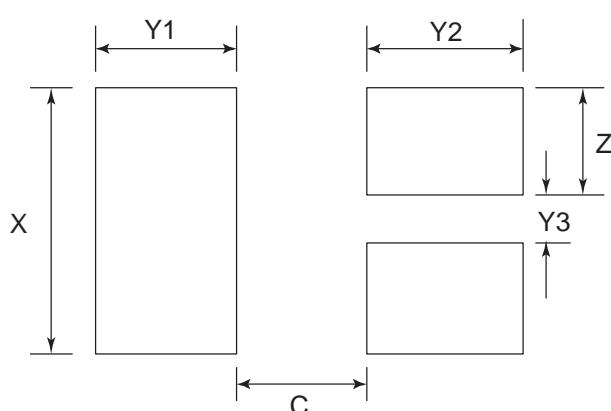
## P-Channel Enhancement Mode MOSFET

### DFN1006-3L Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.45	0.50	0.55	0.018	0.020	0.022
b1	0.10	0.15	0.20	0.004	0.006	0.008
C	0.12	0.15	0.18	0.005	0.006	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
e	0.65 BSC			0.026 BSC		
E	0.55	0.60	0.65	0.022	0.024	0.026
E1	0.15	0.20	0.25	0.006	0.008	0.010
L	0.20	0.25	0.30	0.008	0.010	0.012
L1	0.05 REF			0.0002 REF		

### Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	0.25	0.010
X	0.65	0.024
Y1	0.50	0.020
Y2	0.50	0.020
Y3	0.25	0.010
Z	0.20	0.008