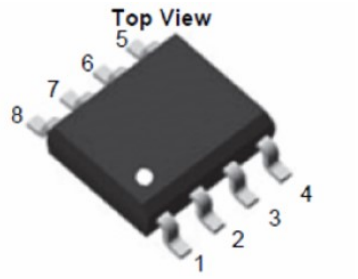
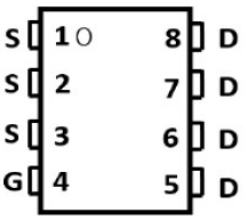
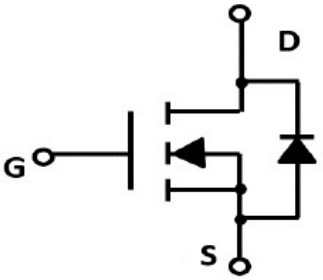
N-Channel Enhancement Mode Field Effect Transistor





SOP－8



Product Summary

- V_{DS} 20V
- I_D 8.5A
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜20mohm
- $R_{DS(ON)}$(at V_{GS}=2.5V) ＜30mohm
- 100% $\triangledown V_{DS}$ Tested

General Description

- Trench Power LV MOSFET technology
- High Power and current handing capability
- High Speed switching

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	20	V
Gate-source Voltage		V_{GS}	±10	V
Drain Current	T_A=25℃	I_D	10	A
	T_A=70℃		8	
Pulsed Drain Current [A]		I_{DM}	45	A
Total Power Dissipation	T_A=25℃	P_D	1.9	W
	T_A=70℃		1.2	W
Thermal Resistance Junction-to-Ambient [B]		$R_{\theta JA}$	66	℃/W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 ~ +150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
FTK10N02S	F2	10N02	4000	8000	64000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±10V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	0.45	0.62	1.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=10A		15	20	mΩ
		V_{GS}=2.5V, I_D=4A		20	26	
Diode Forward Voltage	V_{SD}	I_S=10A,V_{GS}=0V			1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=10V,V_{GS}=0V,f=1MHZ		888		pF
Output Capacitance	C_{oss}			133		
Reverse Transfer Capacitance	C_{rss}			117		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=4.5V,V_{DS}=10V,I_D=6.8A		11.05		nC
Gate-Source Charge	Q_{gs}			1.73		
Gate-Drain Charge	Q_{gd}			3.1		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=4.5V, V_{DS}=10V, I_D=6.8A R_{GEN}=3Ω		7		ns
Turn-on Rise Time	t_r			46		
Turn-off Delay Time	$t_{D(off)}$			30		
Turn-off fall Time	t_f			52		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

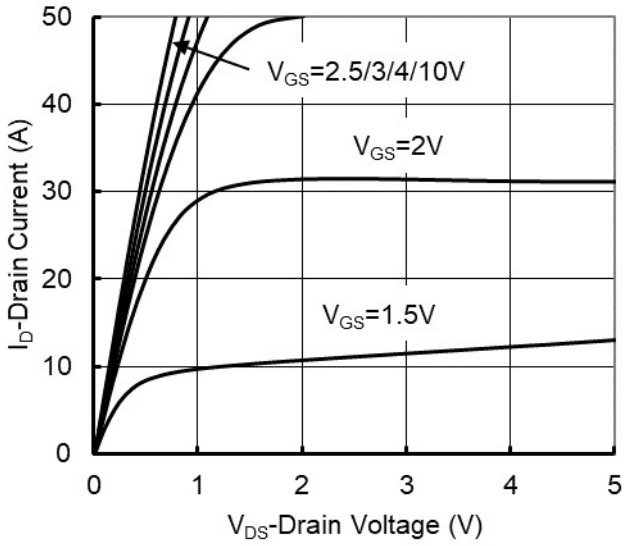


Figure1. Output Characteristics

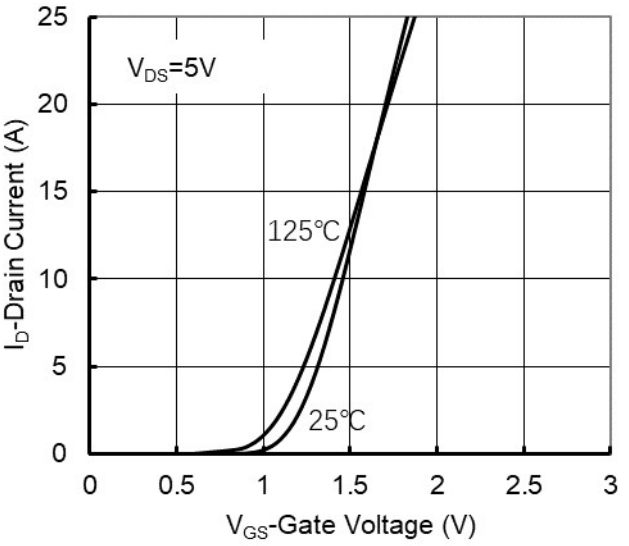


Figure2. Transfer Characteristics

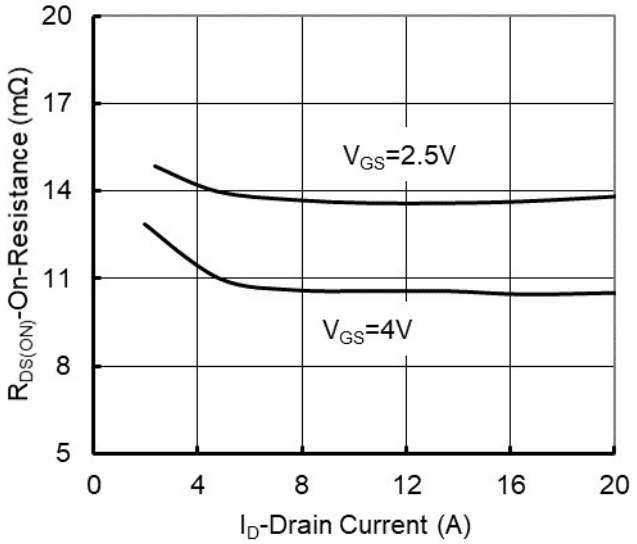


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

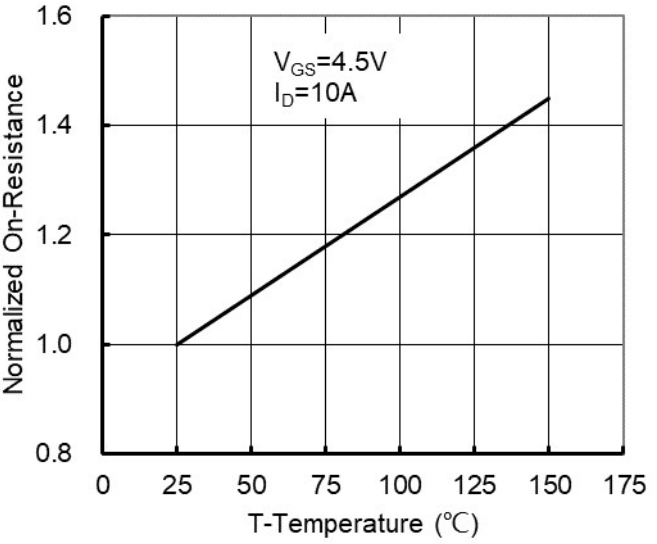


Figure 4: On-Resistance vs. Junction Temperature

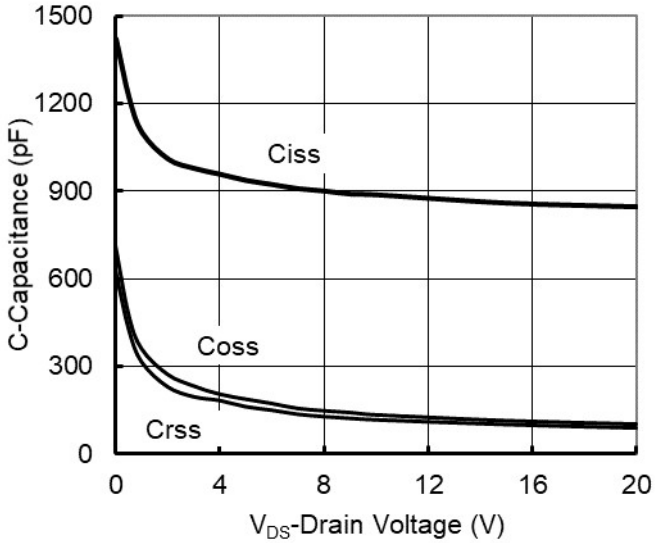


Figure5. Capacitance Characteristics

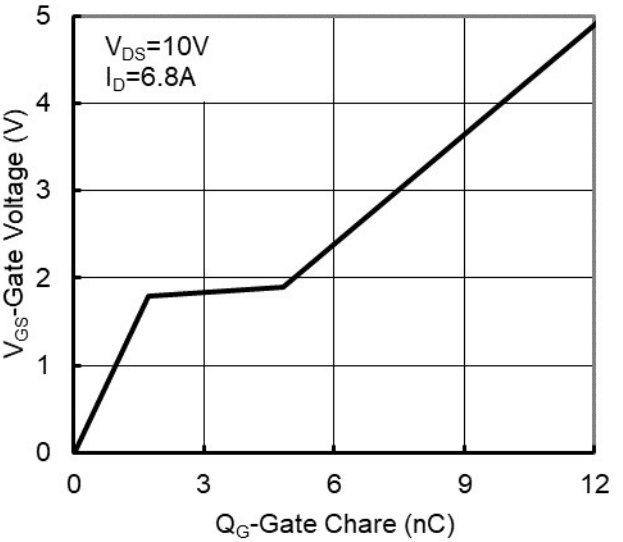


Figure6. Gate Charge

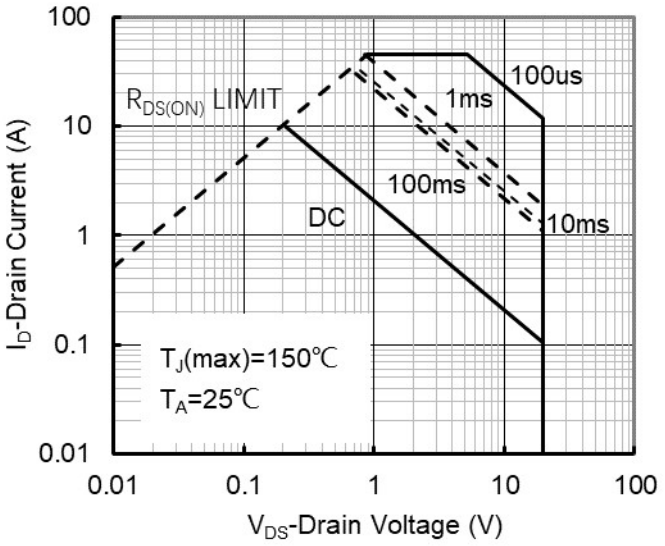


Figure7. Safe Operation Area

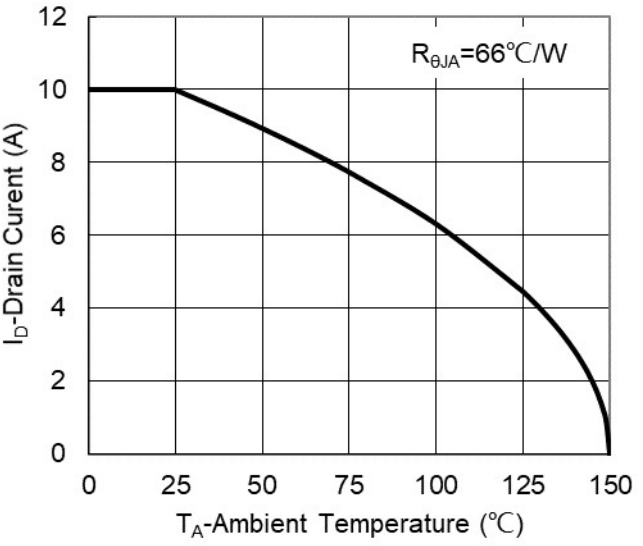


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

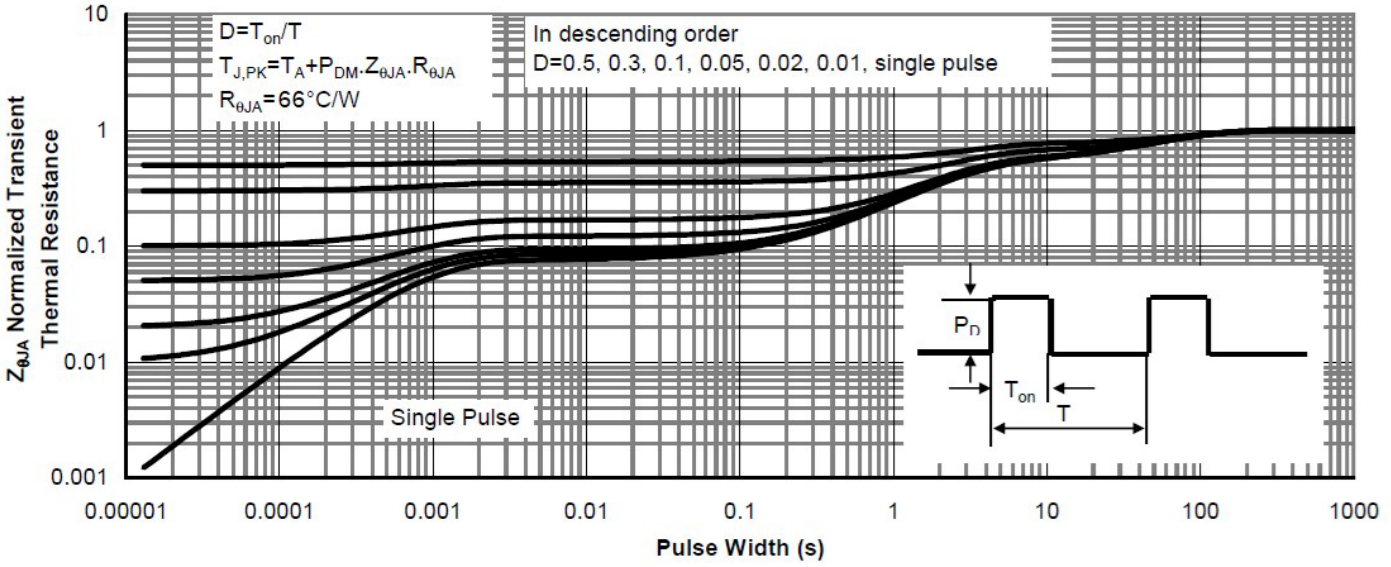
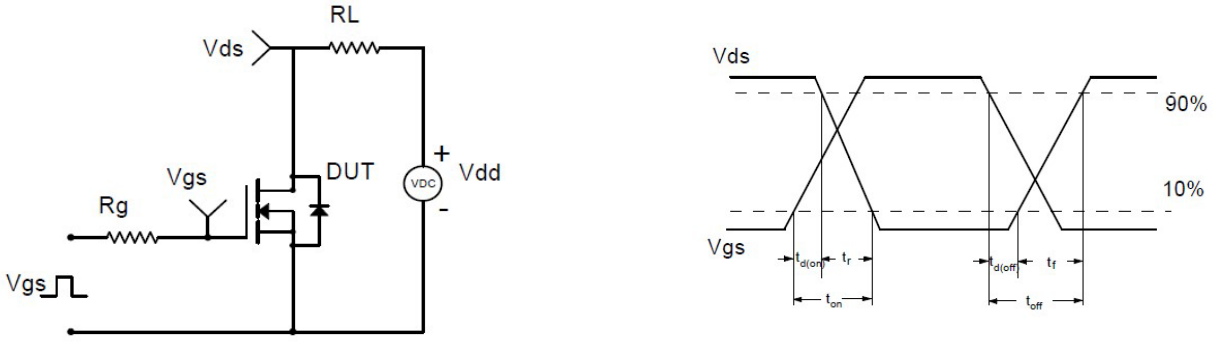
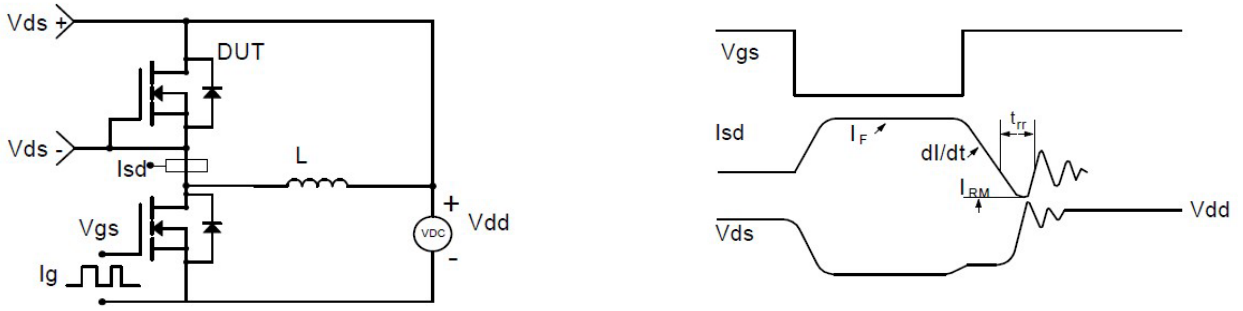


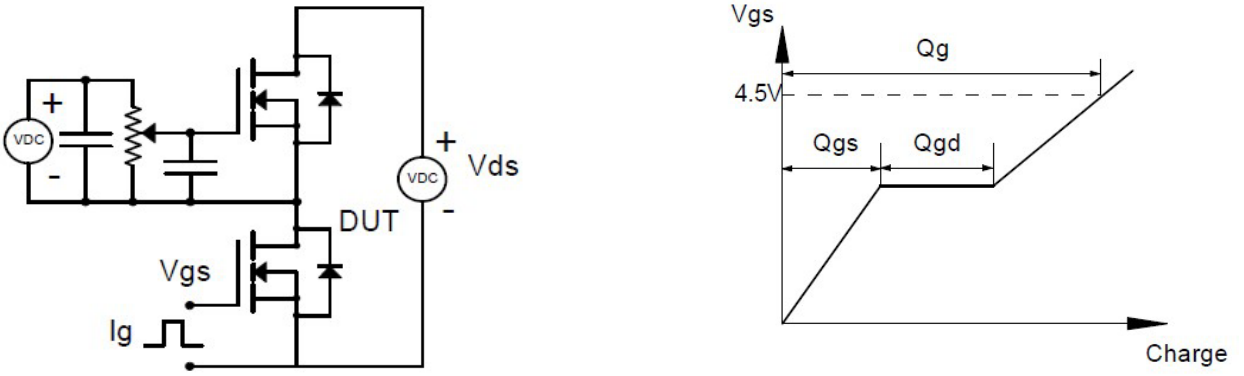
Figure9. Normalized Maximum Transient Thermal Impedance



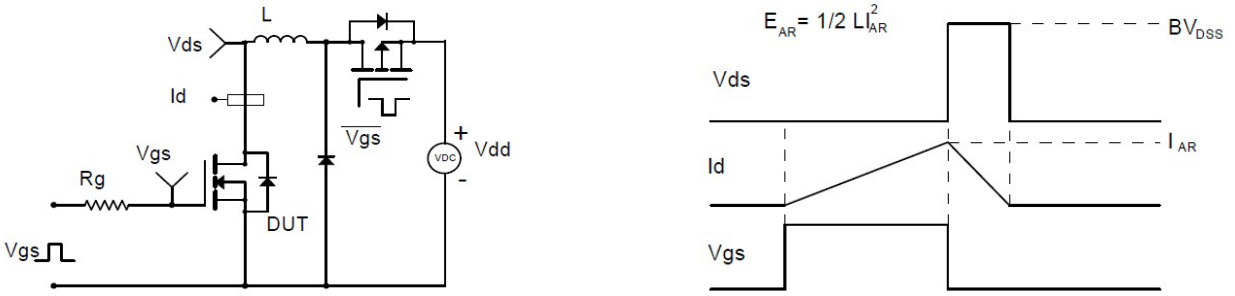
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

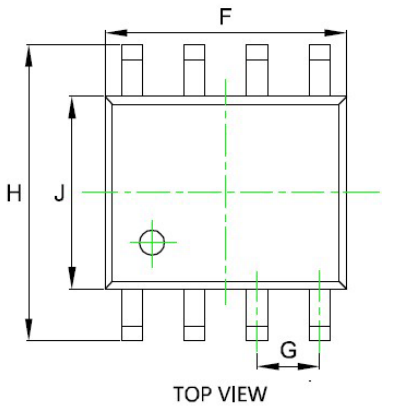


Gate Charge Test Circuit & Waveform

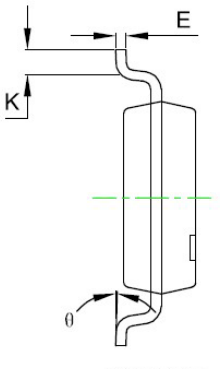


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

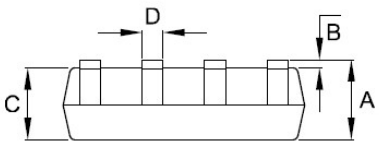
■ SOP-8 Package information



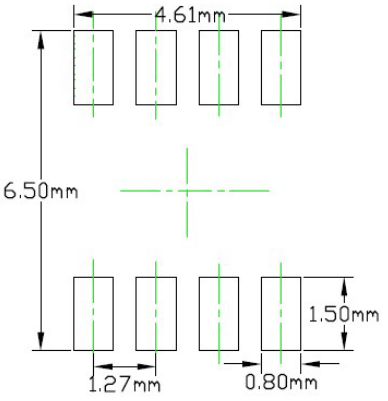
TOP VIEW



SIDE VIEW



SIDE VIEW



Suggested Solder Pad Layout

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°