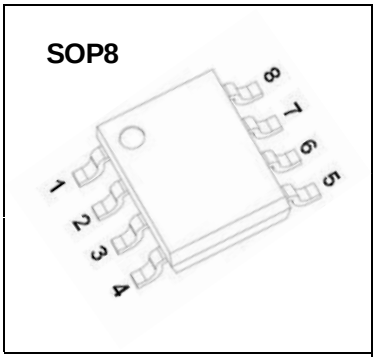
Dual N-Channel MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$MAX	I_D
100V	140mΩ@10V	5A



DESCRIPTION

The FTK05N10S10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge .This device is suitable for use in a wide variety of applications.

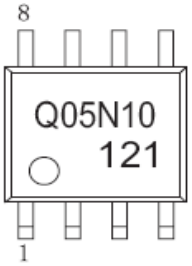
FEATURES

- Lead free product is acquired
- Special process technology for high ESD capability
- High density cell design for ultra low $R_{DS(on)}$
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

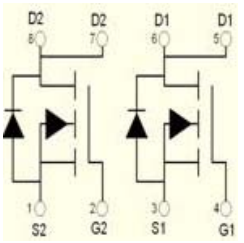
APPLICATION

- Power switching application
- Hard switching and high frequency circuits
- Uninterruptible power supply

MARKING:



Equivalent Circuit



Maximum ratings (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain- SourceVoltage	V_{DS}	100	V
Gate- Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	5	A
Pulsed Drain Current **(note 1)**	I_{DM}	24	A
Power Dissipation (note 1)	P_D	1.4	W
Thermal Resistance from Junction to Ambient **(note 2)**	$R_{\theta JA}$	89	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	- 55~ +150	℃

Electrical characteristics (T_a=25℃ unless otherwise noted)

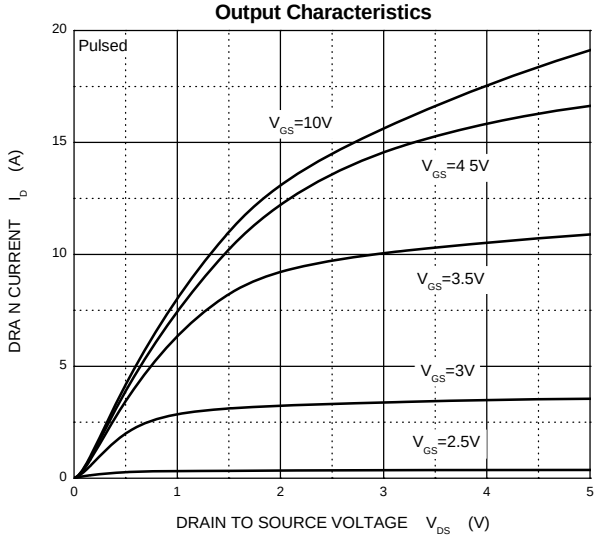
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC CHARACTERISTICS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D=250μA	100			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =100V,V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V			±100	nA
Gate threshold voltage **(note 3)**	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	1		2	V
Drain-source on-resistance **(note 3)**	$R_{DS(on)}$	V_{GS} =10V, I_D=5A			140	mΩ
Forward transconductance **(note 3)**	g_{FS}	V_{DS} =5V, I_D=2.9A		8		S
Diode forward voltage **(note 3)**	V_{SD}	I_S=5A, V_{GS} = 0V			1.2	V
DYNAMIC CHARACTERISTICS (note 4)						
Input capacitance	C_{iss}	V_{DS} =25V,V_{GS} =0V,f=1MHz		690		pF
Output capacitance	C_{oss}			120		pF
Reverse transfer capacitance	C_{rss}			90		pF
SWITCHING CHARACTERISTICS (note 4)						
Turn-on delay time	$t_{d(on)}$	V_{GS}=10V,V_{DS}=30V, R_{GEN}=2.5Ω, I_D=2A, R_L=15Ω		11		ns
Turn-on rise time	t_r			7.4		ns
Turn-off delay time	$t_{d(off)}$			35		ns
Turn-off fall time	t_f			9.1		ns
Total gate charge	Q_g	V_{DS} =30V,V_{GS} =10V,I_D =3A		15.5		nC
Gate-source Charge	Q_{gs}			3.2		nC
Gate-drain Charge	Q_{gd}			4.7		nC

Notes :

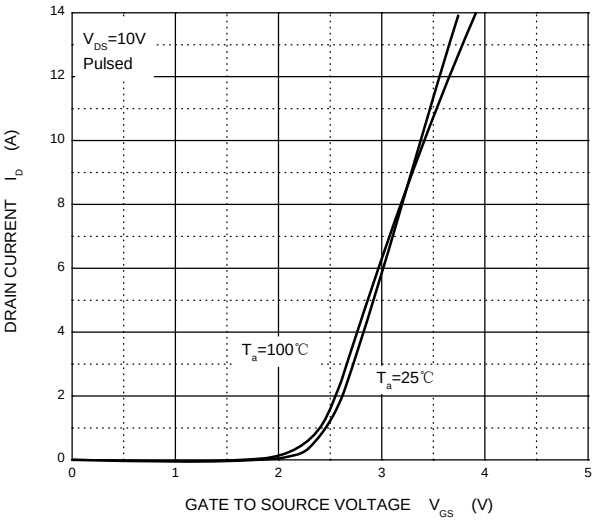
1. Repetitive rating : Pulse width limited by junction temperature.
2. Surface mounted on FR4 board ≤t10s.
3. Pulse Test : Pulse Width≤300μs, Duty Cycle≤2%.
4. Guaranteed by design, not subject to producting.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

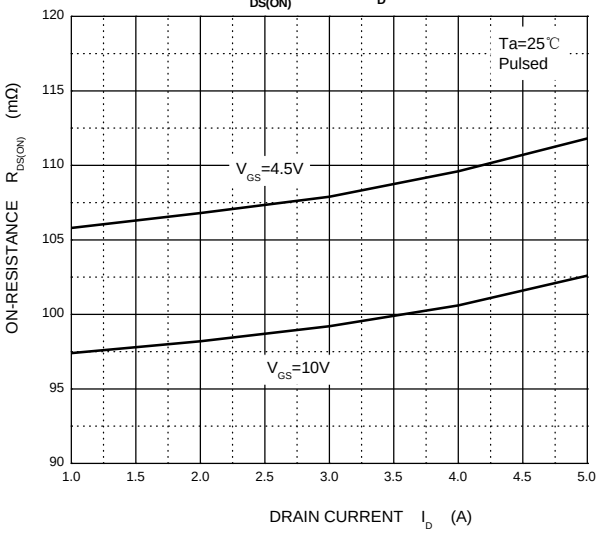
Output Characteristics



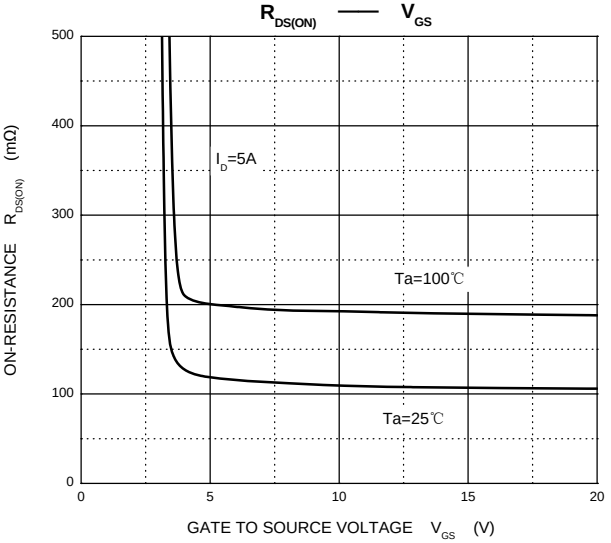
Transfer Characteristics



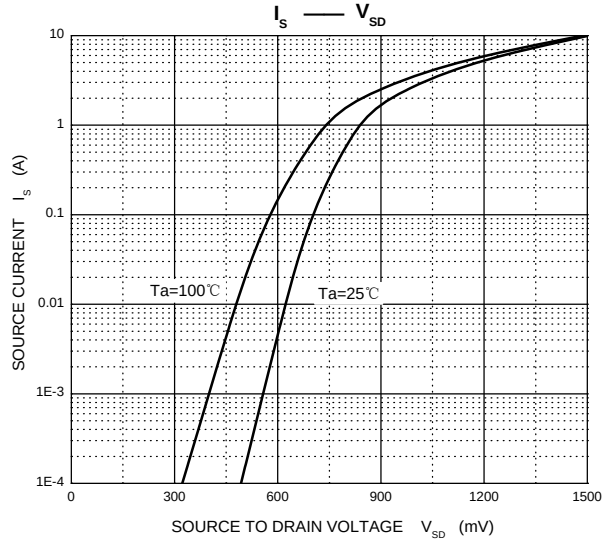
$R_{DS(ON)}$ —— I_D



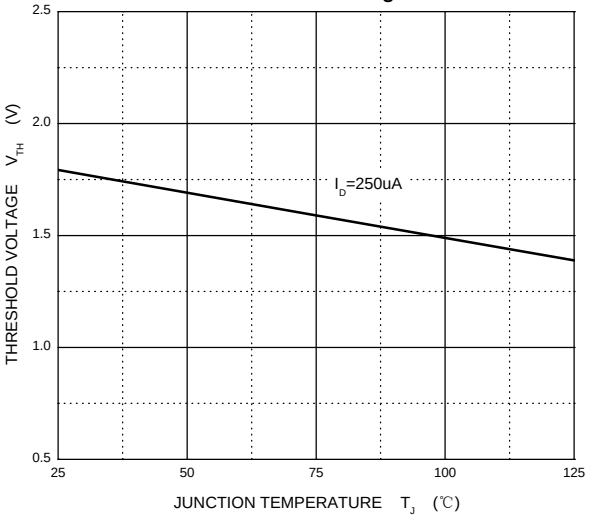
$R_{DS(ON)}$ —— V_{GS}



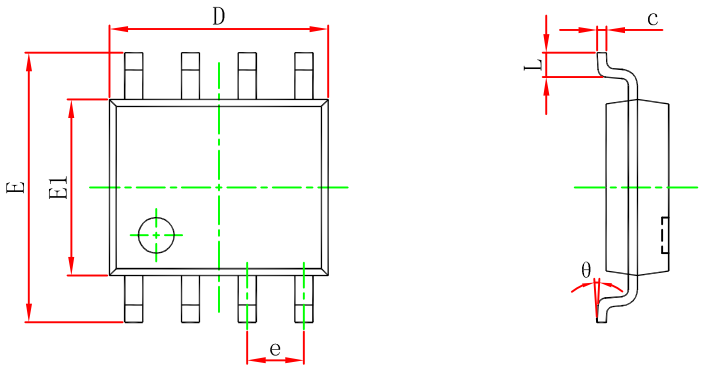
I_S —— V_{SD}



Threshold Voltage

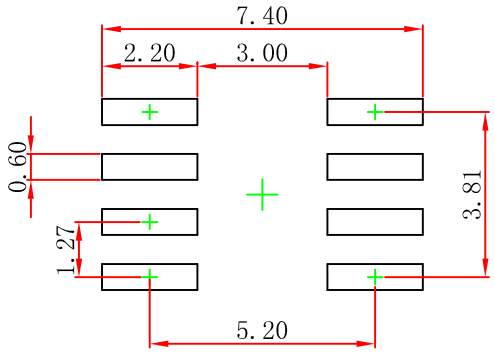


SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	---	1.750	---	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.500	0.049	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOP-8 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.