

12 Amps, 650 Volts N-CHANNEL MOSFET

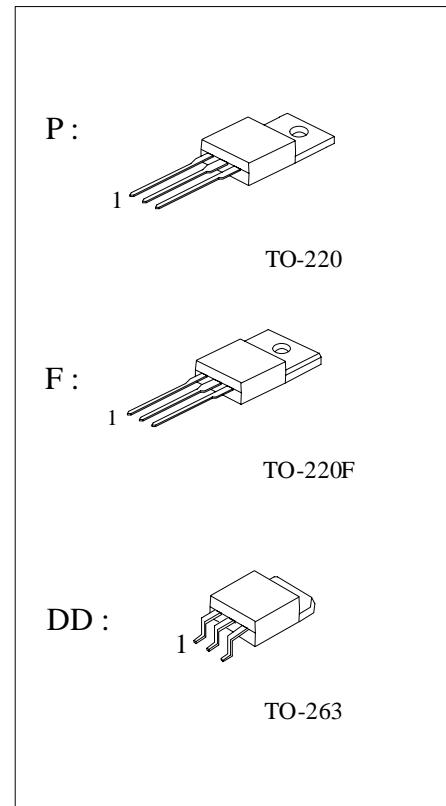
■ DESCRIPTION

These N-Channel enhancement mode power field effect Transistors are produced using planar stripe, DMOS technology.

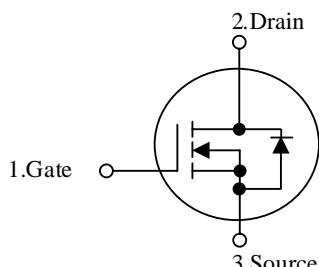
This advanced technology has been especially tailored to minimize on - state resistance , provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode .These devices are well suited for high efficiency switch mode power supply, electronic lamp ballasts based on half bridge topology.

■ FEATURES

- * $R_{DS(ON)} = 0.8\Omega @ V_{GS} = 10V$
- * Fast switching capability
- * Avalanche energy tested
- * Improved dv/dt capability, high ruggedness



■ SYMBOL



■ ORDERING INFORMATION

Order Number	Package	Pin Assignment			Packing
		1	2	3	
FTK12N65P	TO-220	G	D	S	Tube
FTK12N65F	TO-220F	G	D	S	Tube
FTK12N65DD	TO-263	G	D	S	Reel & Taping

Note: Pin Assignment: G: Gate D: Drain S: Source



■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMET		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V _{DSS}	650	V
Gate-Source Voltage		V _{GSS}	±30	V
Avalanche Current (Note 1)		I _{AR}	12	A
Continuous Drain Current	T _C = 25°C	I _D	12	A
	T _C = 100°C		6.5	
Pulsed Drain Current (Note 1)		I _{DM}	48	A
Avalanche Energy	Single Pulse(Note 2)	E _{AS}	790	mJ
	Repetitive Limited by T _{J(MAX)}	E _{AR}	24	mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.5	V/ns
Power Dissipation (TO-220,TO-263/ TO-220F)	T _C = 25°C	P _D	225 / 51	W
	Derate above 25°C		1.25 / 0.38	W / °C
Junction Temperature		T _J	+150	°C
Operating and Storage Temperature		T _{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Junction-to-Ambient		θ _{JA}			62.5	°C / W
Junction-to-Case	TO-220, TO-263	θ _{Jc}			0.56	
	TO-220F	θ _{Jc}			2.43	

■ ELECTRICAL CHARACTERISTICS (T_C = 25°C , unless Otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	650			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} = 650V, V _{GS} = 0V			10	μA
Gate-Body Leakage Current	Forward	I _{GSSF}	V _{GS} = 30V, V _{DS} = 0V			nA
	Reverse	I _{GSRR}	V _{GS} = -30V, V _{DS} = 0V			-100 nA
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} / ΔT _J	I _D = 250μA, Referenced to 25°C		0.7		V / °C
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	2.0		4.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 6.0A			0.8	Ω
Forward Transconductance	g _F	V _{DS} = 40V, I _D = 6.0A (Note 4)		8.7		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz		1480		pF
Output Capacitance	C _{OSS}			200		pF
Reverse Transfer Capacitance	C _{rss}			25		pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 350V , I _D = 12A , R _G = 25Ω (Note 4,5)		30		ns
Turn-On Rise Time	t _R			115		ns
Turn-Off Delay Time	t _{D(OFF)}			95		ns
Turn-Off Fall Time	t _F			85		ns
Total Gate Charge	Q _G	V _{DS} = 520V, I _D = 12A V _{GS} = 10V (Note 4,5)		42		nC
Gate-Source Charge	Q _{GS}			8.6		nC
Gate-Drain Charge	Q _{GD}			21		nC



FTK12N65P/F/DD

■ ELECTRICAL CHARACTERISTICS (T_J = 25°C , unless Otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _S = 12A			1.4	V
Maximum Continuous Drain-Source Diode Forward Current	I _S				12	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				48	A
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, I _S = 12A,		380		ns
Reverse Recovery Charge	Q _{RR}	dI _F /dt = 100 A/μs (Note 4)		3.5		μC

Note:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 10.0mH, I_{AS} = 12A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 12A, di/dt ≤ 200A/ μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

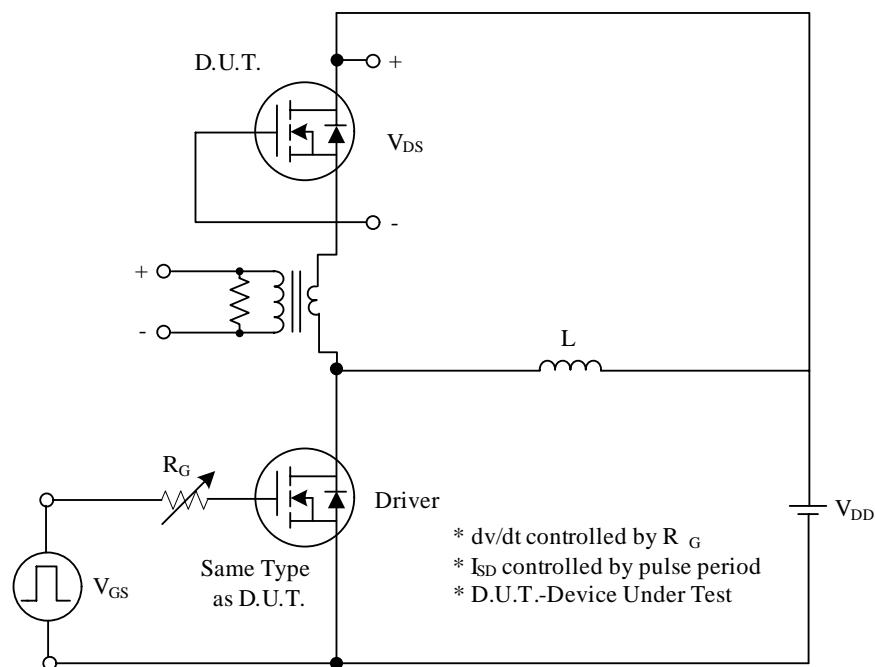


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

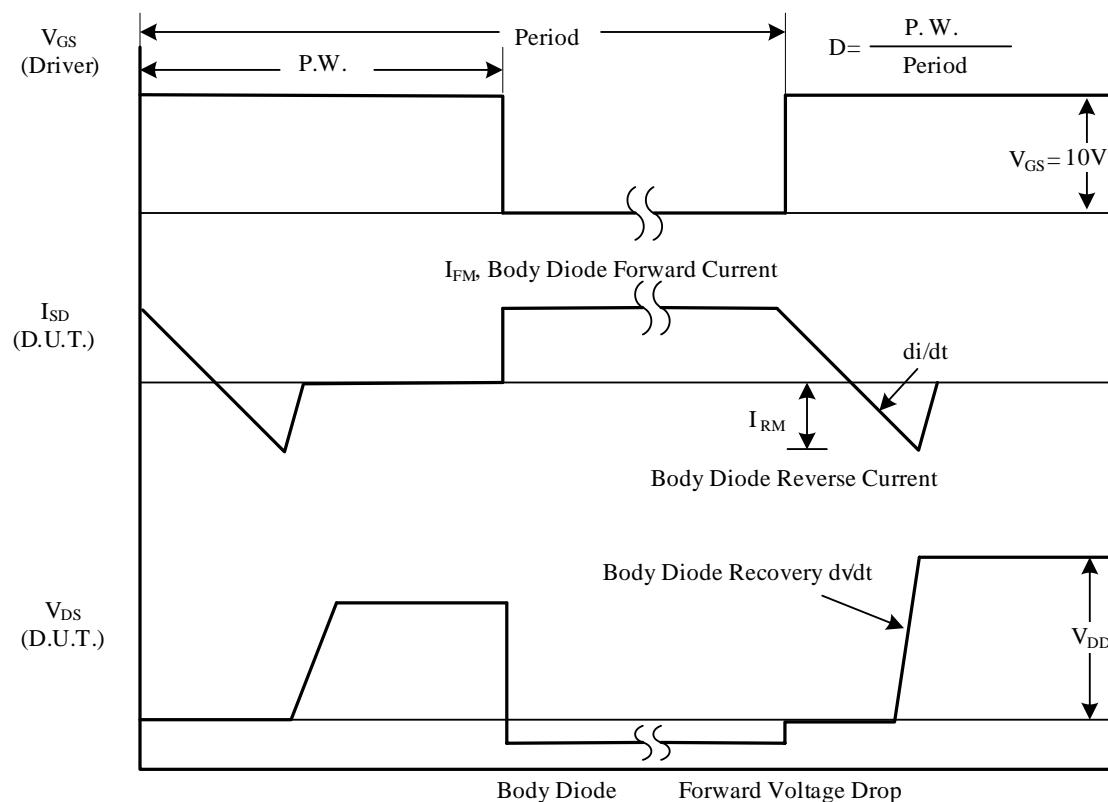


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

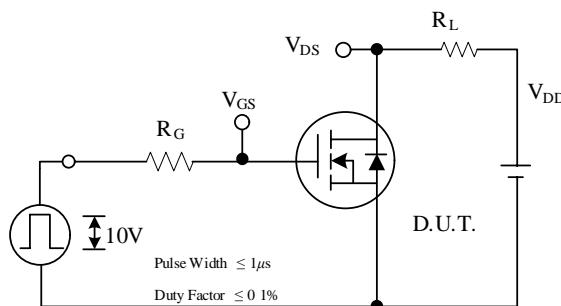


Fig. 2A Switching Test Circuit

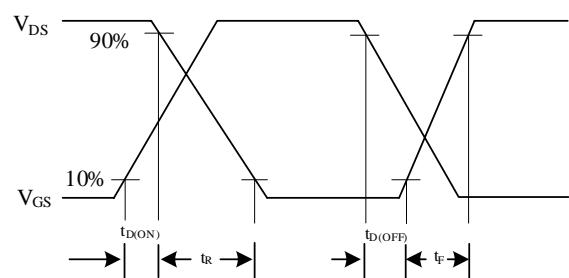


Fig. 2B Switching Waveforms

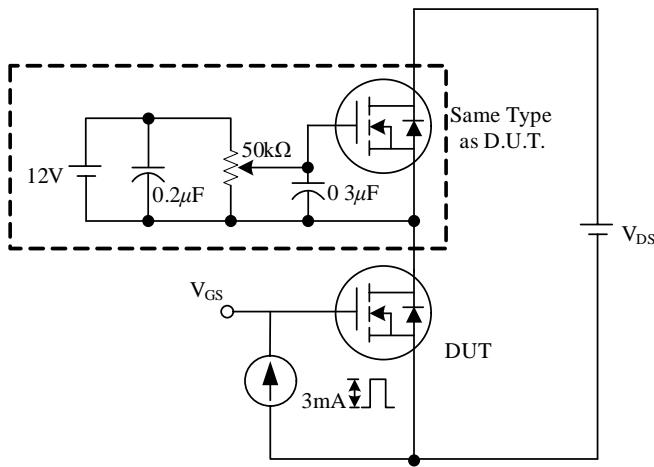


Fig. 3A Gate Charge Test Circuit

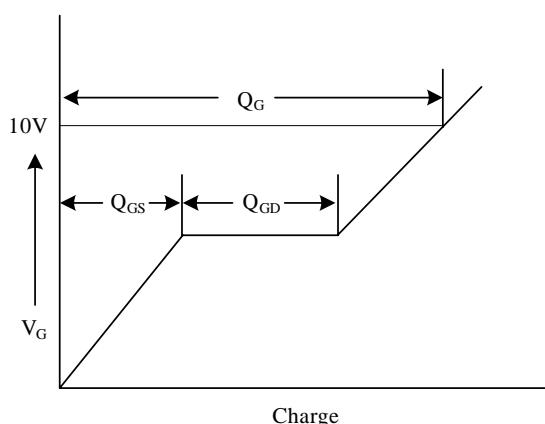


Fig. 3B Gate Charge Waveform

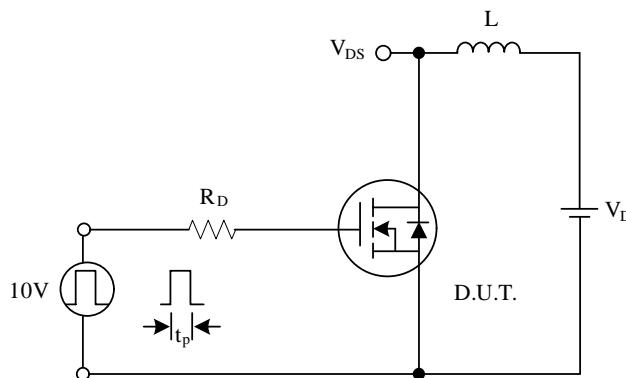


Fig. 4A Unclamped Inductive Switching Test Circuit

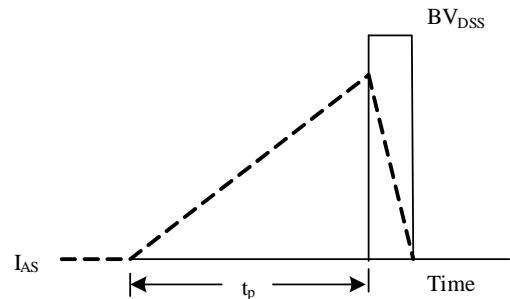


Fig. 4B Unclamped Inductive Switching Waveforms

■ TYPICAL CHARACTERISTICS

