N-CHANNEL QUET MOSFET
## 500 V , 9 A, 800 mΩ

Features

- 9 A, 500 V, $R_{DS(on)}$ = 800 mΩ (Max.) @ V_{GS} = 10 V, I_D = 4.5 A
- Low Gate Charge (Typ. 28 nC)
- Low Crss (Typ. 24 pF)
- 100% Avalanche Tested

Description

This N-Channel enhancement mode power MOSFET is produced using **First silicon's** proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

D²-PAK
(TO-263)
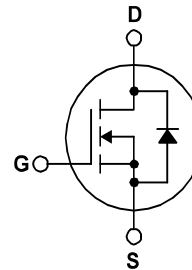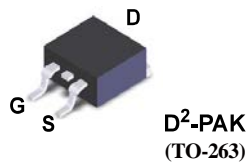
Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FTK9N50DD	Unit
V_{DSS}	Drain-Source Voltage		500	V
I_D	Drain Current - Continuous (T_C = 25°C)		9	A
	- Continuous (T_C = 100°C)		5.4	A
I_{DM}	Drain Current - Pulsed	(Note 1)	36	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	360	mJ
I_{AR}	Avalanche Current	(Note 1)	9	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	13.5	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)		135	W
	- Derate above 25°C		1.07	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FTK9N50DD	Unit
$R_{θJC}$	Thermal Resistance, Junction-to-Case, Max.	0.93	°C/W
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FTK9N50	**FTK9N50DD**	**TO-263**	330 mm	24 mm	800 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	500	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.57	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 400 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4.5 A	--	0.65	0.8	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 4.5 A	--	6.5	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	790	1030	pF
C_{oss}	Output Capacitance		--	130	170	pF
C_{rss}	Reverse Transfer Capacitance		--	24	30	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 9 A, R_G = 25 Ω	--	18	45	ns
t_r	Turn-On Rise Time		--	65	140	ns
$t_{d(off)}$	Turn-Off Delay Time		--	93	195	ns
t_f	Turn-Off Fall Time	(Note 4)	--	64	125	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 9 A, V_{GS} = 10 V	--	28	35	nC
Q_{gs}	Gate-Source Charge		--	4	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4)	--	15	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	9	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	36	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 9 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 9 A, dI_F / dt = 100 A/μs	--	335	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.95	--	μC

NOTES:

1. Repetitive Rating : Pulse width limited by maximum junction temperature.

2. L = 8 mH, I_{AS} = 9 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.

3. $I_{SD} \leq$ 9 A, di/dt $\leq$ 200 A/μs, $V_{DD} \leq BV_{DSS}$, starting T_J = 25°C.

4. Essentially independent of operating temperature.

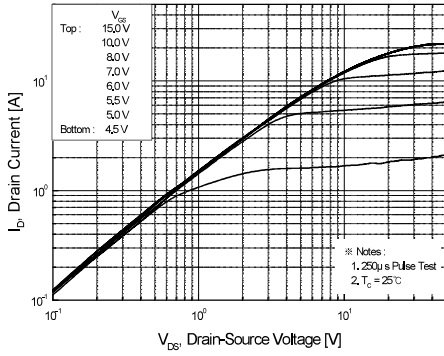# ■ TYPICAL CHARACTERISTICS

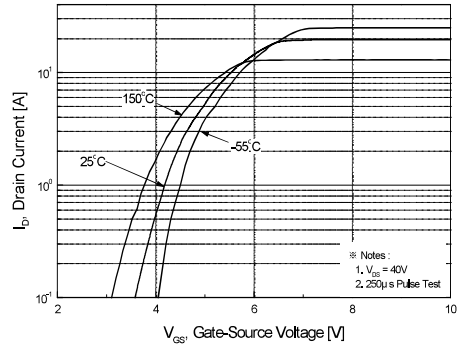Figure 1. On-Region Characteristics
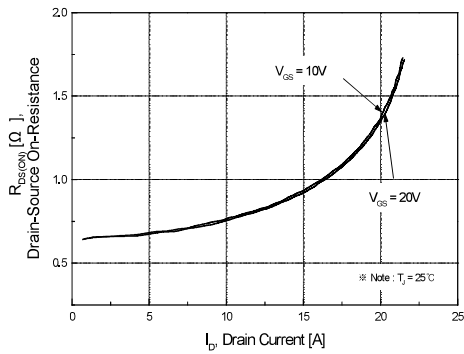

Figure 2. Transfer Characteristics

Figure 3. On-Resistance Variation vs
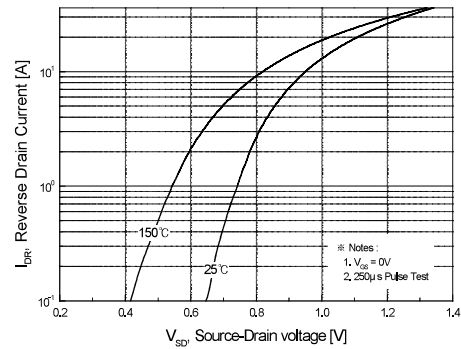Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage
Variation with Source Current
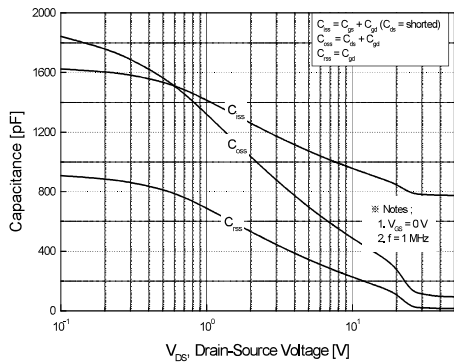and Temperature
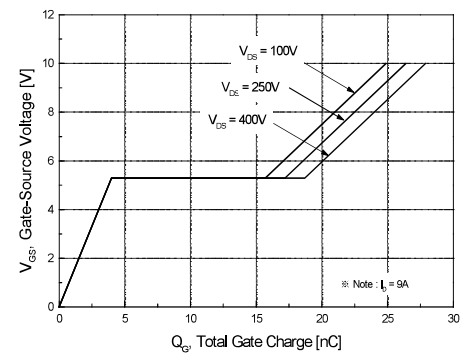

Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics
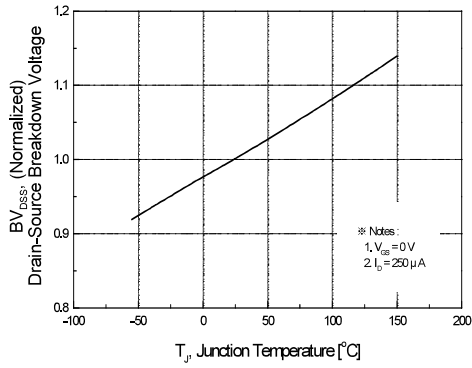
Typical Characteristics (Continued)

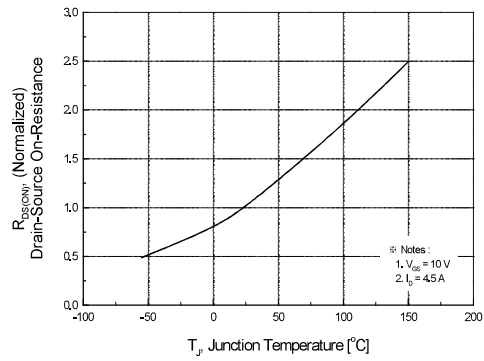Figure 7. Breakdown Voltage Variation
vs Temperature

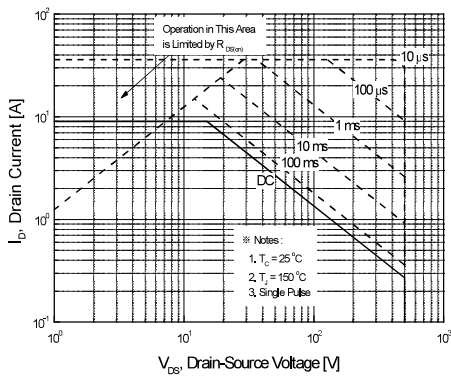Figure 8. On-Resistance Variation
vs Temperature

Figure 9. Maximum Safe Operating Area

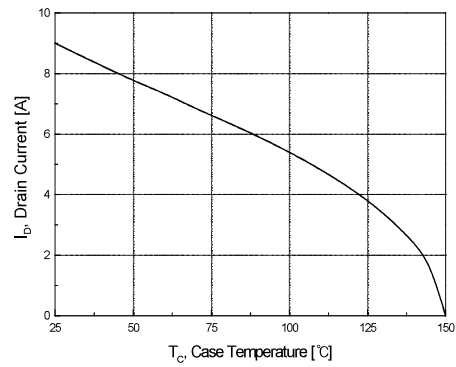Figure 10. Maximum Drain Current
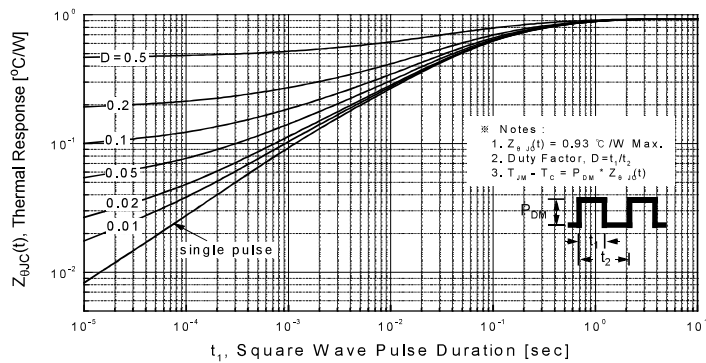vs Case Temperature

Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

Charge
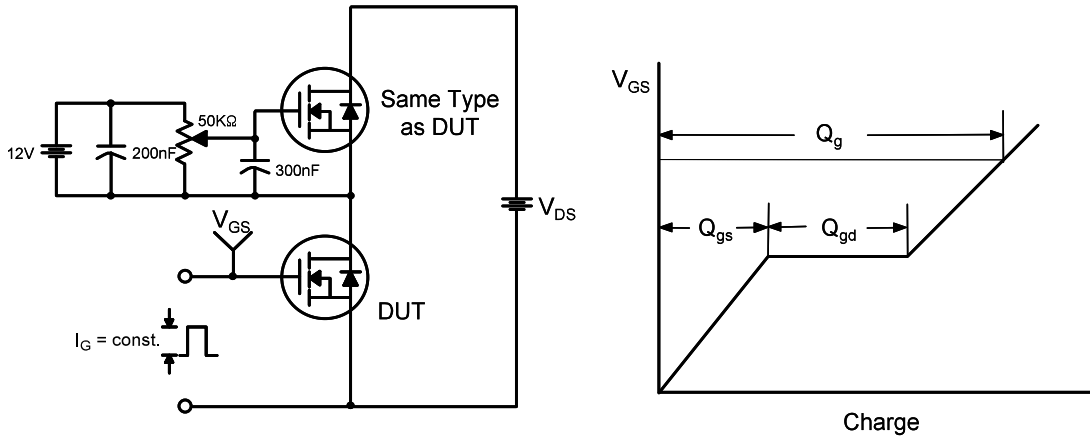
Figure 13. Resistive Switching Test Circuit & Waveforms
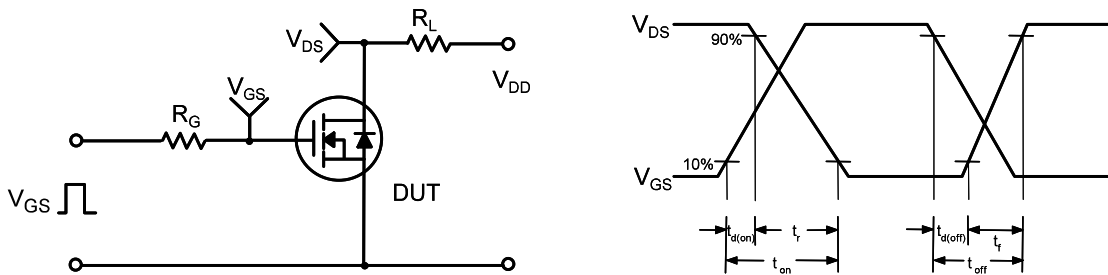
Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \; \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$
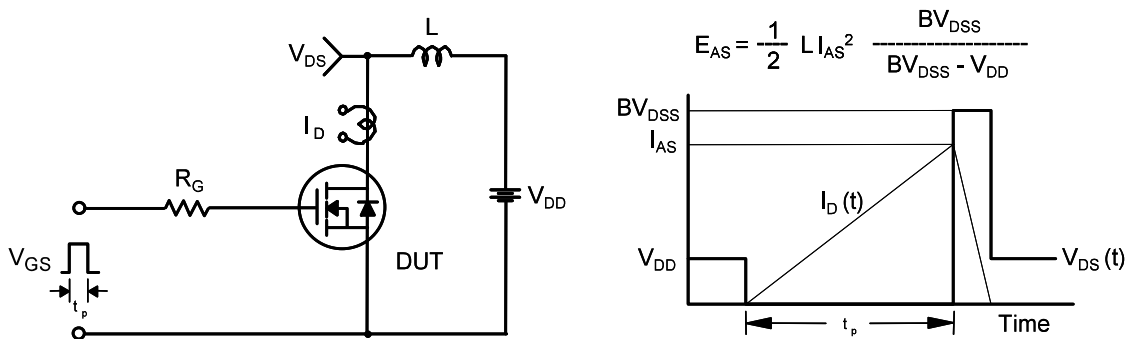
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS} (Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD} (DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS} (DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode Forward Voltage Drop

10.67
9.65

A

1.68
1.00

4

9.65
8.38

1.78 MAX

2

1

3

(2.12)

1.78
1.14

0.99
0.51

5.08

⊕ 0.25 Ⓜ B AⓂ

12.70

9.45

10.00

(6.40)

3.80

1.05

5.08

LAND PATTERN RECOMMENDATION
UNLESS NOTED, ALL DIMS TYPICAL

6.22 MIN

4

6.86 MIN

2

3

1

B

4.83
4.06

1.65
1.14

15.88
14.61

SEE
DETAIL A

NOTES: UNLESS OTHERWISE SPECIFIED
A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) REFERENCE JEDEC, TO-263, VARIATION AB.
C) DIMENSIONING AND TOLERANCING PER
   ANSI Y14,5M – 1994.
D) LOCATION OF THE PIN HOLE MAY VARY
   (LOWER LEFT CORNER, LOWER CENTER
   AND CENTER OF THE PACKAGE).
E) LANDPATTERN RECOMMENDATION PER IPC
   TO254P1524X482-3N
F) FILENAME: TO263A02REV6

GAGE PLANE

0.74
0.33

8°
0°

0.25

0.25 MAX

2.79
1.78

8°
0°

△ 0.10 B

(5.38)

SEATING
PLANE

DETAIL A, ROTATED 90°
SCALE: 2X