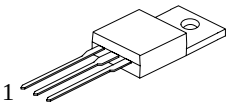
11Amps, 650Volts N-Channel Super Juction MOS-FET

Product Summary

V_{DS} @ $T_{j,max}$	650V
$R_{DS(on),max}$	0.37Ω
I_{DM}	30A
$Q_{g,typ}$	28nC

P :



TO-220

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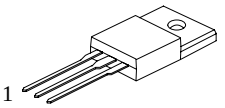

TO-220F

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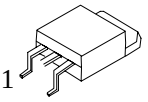

TO-252

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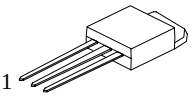


TO - 251

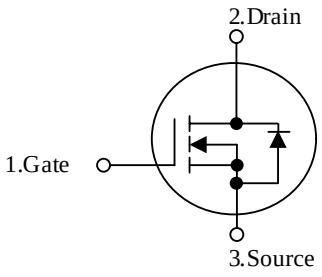
DESCRIPTION

FTK11NS65 Power MOS FET is fabricated using advanced super junction technology. The resulting device has extremely low on resistance, making it especially suitable for applications which require superior power density and outstanding efficiency.

FEATURES

- □ Ultra fast body diode
- □ Ultra low $R_{DS(on)}$
- □ Ultra low gate charge (typ. Q_g = 28nC)
- □ 100% UIS tested
- □ RoHS compliant

SYMBOL



Applications

- □ Power faction correction (PFC).
- □ Switched mode power supplies (SMPS).
- □ Uninterruptible power supply (UPS).

ORDERING INFORMATION

Order Number	Package	Pin Assignment			Packing
		1	2	3	
FTK11NS65P	TO-220	G	D	S	Tube
FTK11NS65F	TO-220F	G	D	S	Tube
FTK11NS65D	TO-252	G	D	S	Tube
FTK11NS65I	TO-251	G	D	S	Reel & Taping

Note: Pin Assignmen: G: Gate D: Drain S: Source

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DSS}	650	V
Continuous drain current (T_C = 25°C)	I_D	11	A
(T_C = 100°C)		7	A
Pulsed drain current [1]	I_{DM}	30	A
Gate - Source voltage	V_{GSS}	± 30	V
Avalanche energy, single pulse [2]	E_{AS}	350	mJ
Avalanche energy, repetitive [1]	E_{AR}	12.5	mJ
Avalanche current, repetitive [1]	I_{AR}	11	A
Power Dissipation (T_C = 25°C)	P_D	83	W
- Derate above 25°C		0.67	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C
Continuous diode forward current	I_S	11	A
Diode pulse current	$I_{S,pulse}$	30	A

Thermal CharacteristicsTO-220/TO-251/TO-252

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62	°C/W

Thermal Characteristics TO-220F

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4.3	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	80	°C/W

Electrical Characteristics

T_c = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0 V, I_D=0.25 mA	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.25mA	2	3.5	5	V
Drain cut-off current	I_{DSS}	V_{DS}=650 V, V_{GS}=0 V,	-	-	1	μA
Gate leakage current, Forward	I_{GSSF}	V_{GS}=30 V, V_{DS}=0 V	-	-	100	nA
Gate leakage current, Reverse	I_{GSSR}	V_{GS}=-30 V, V_{DS}=0 V	-	-	-100	nA
Drain -source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=5.5A T_j = 25°C T_j = 150°C	- - -	 0.33 0.69	 037 -	Ω
Gate resistance	R_G	f=1 MHz, open drain	-	0.9	-	Ω
Dynamic characteristics						
Input capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	-	1040	-	pF
Output capacitance	C_{oss}		-	780	-	
Reverse transfer capacitance	C_{rss}		-	10	-	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 380V, I_D = 5.5A, R_G = 4.7Ω, V_{GS}=10V	-	16	-	ns
Rise time	t_r		-	14	-	
Turn-off delay time	$t_{d(off)}$		-	40	-	
Fall time	t_f		-	5	-	
Gate charge characteristics						
Gate to source charge	Q_{gs}	V_{DD}=480 V, I_D=5.5A, V_{GS}=0 to 10 V	-	6	-	nC
Gate to drain charge	Q_{gd}		-	13	-	
Gate charge total	Q_g		-	28	-	
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V
Reverse diode characteristics						
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=5.5A	-	-	1.4	V
Reverse recovery time	t_{rr}	V_R=50 V, I_F=11A, dI_F/dt=100 A/μs	-	430	-	ns
Reverse recovery charge	Q_{rr}		-	3.6	-	μC
Peak reverse recovery current	I_{rrm}		-	15	-	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I_{AS} = 3.5A, V_{DD} = 60V, R_G = 25Ω, Starting T_J = 25°C

Typical Characteristics

Figure 1. On-Region Characteristics

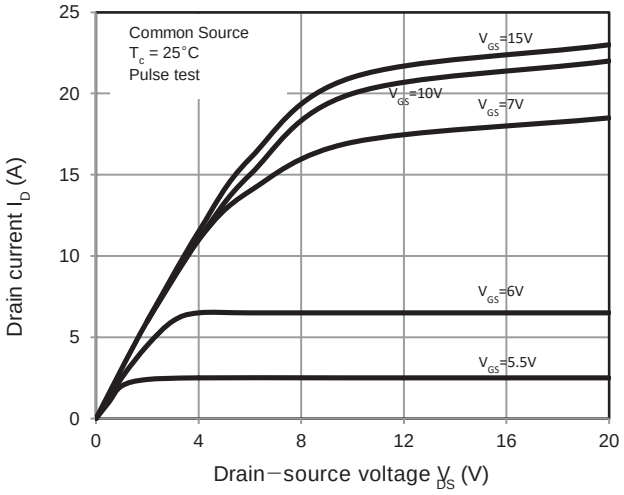


Figure 2. Transfer Characteristics

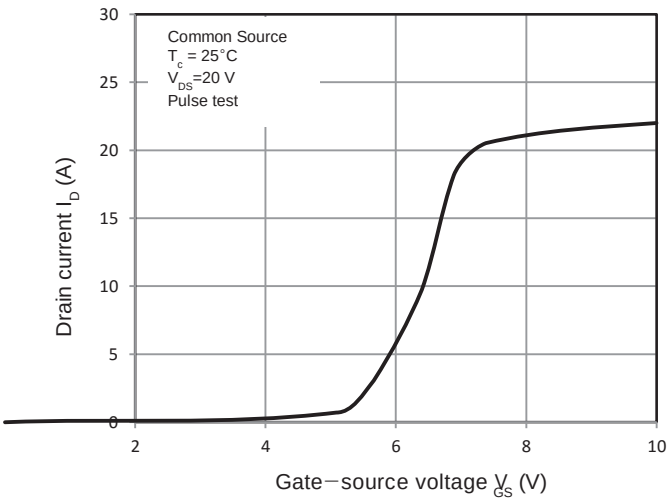


Figure 3. On-Resistance Variation vs. Drain Current

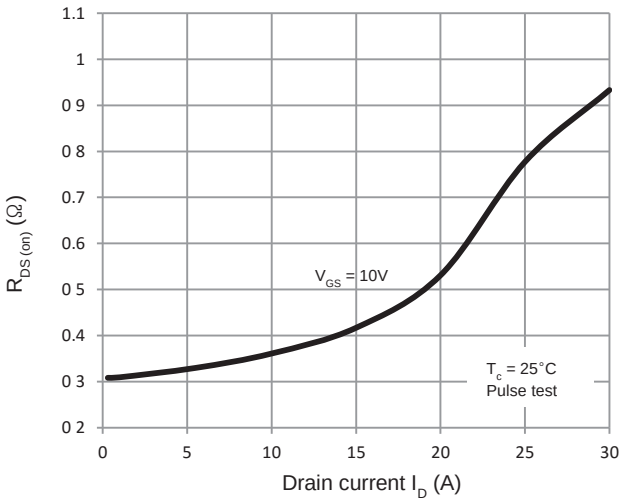


Figure 4. Threshold Voltage vs. Temperature

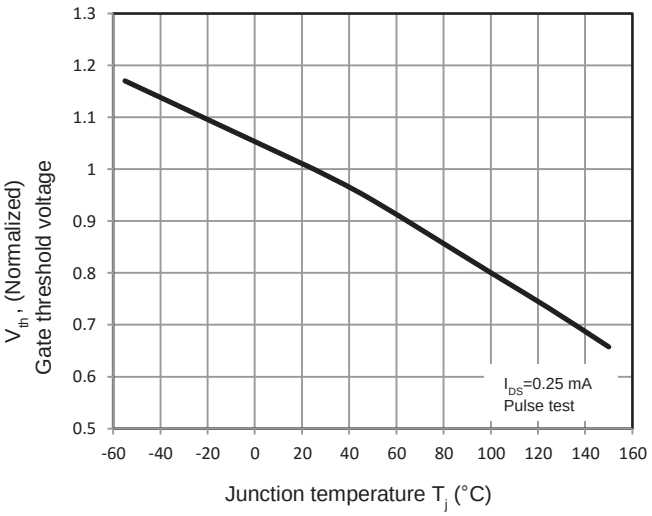


Figure 5. Breakdown Voltage vs. Temperature

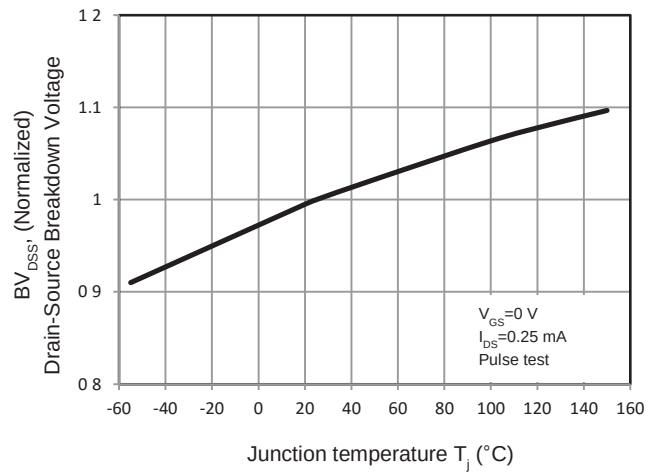


Figure 6. On-Resistance vs. Temperature

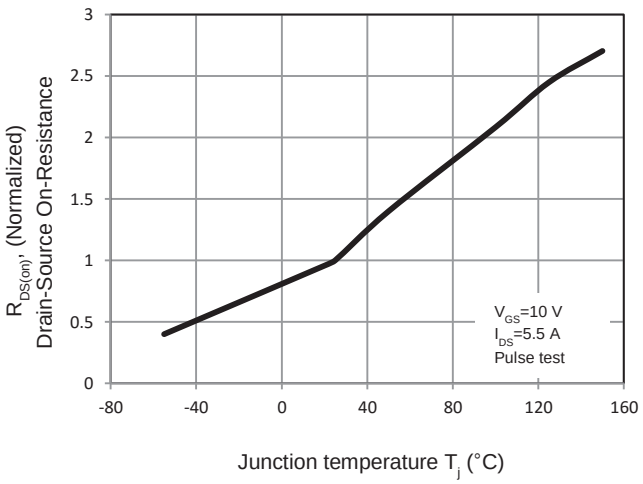


Figure 7. Capacitance Characteristics

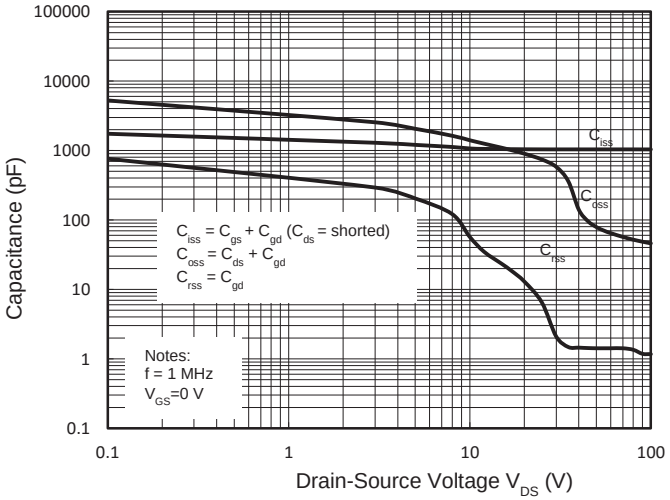


Figure 8. Gate Charge Characteristics

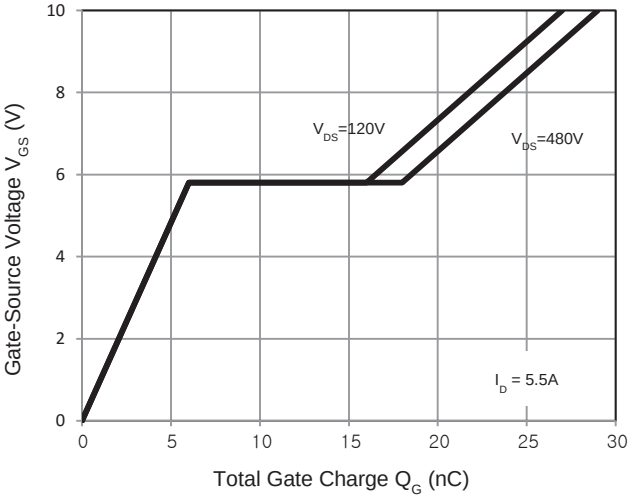


Figure 9. Maximum Safe Operating Area

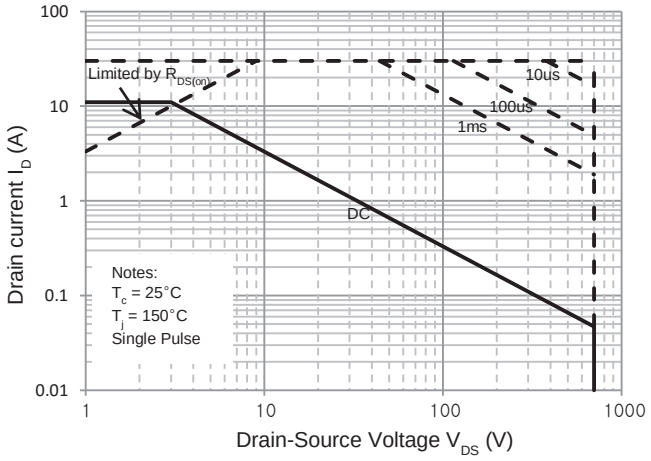


Figure 10. Power Dissipation vs. Temperature

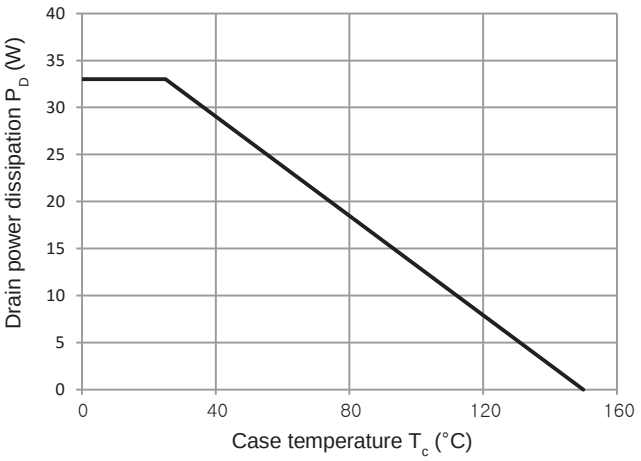
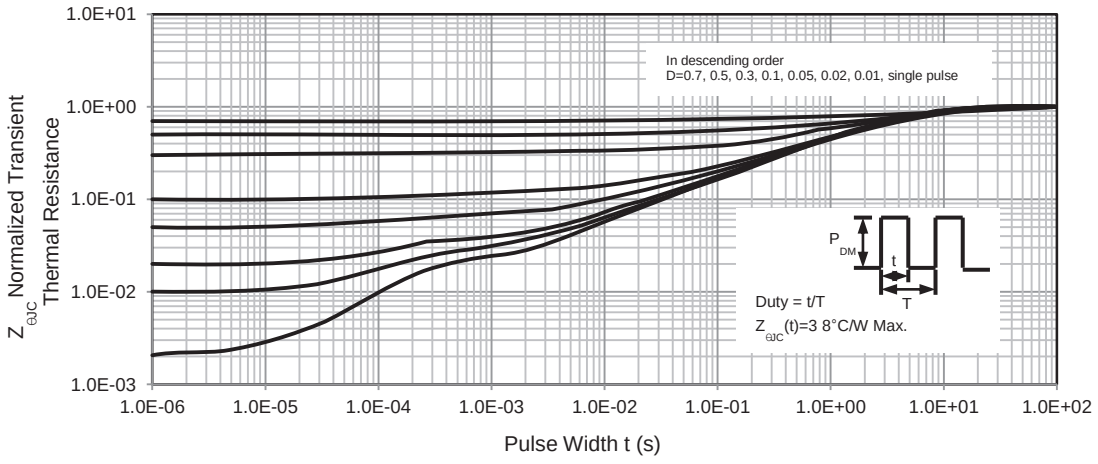


Figure 11. Transient Thermal Response Curve



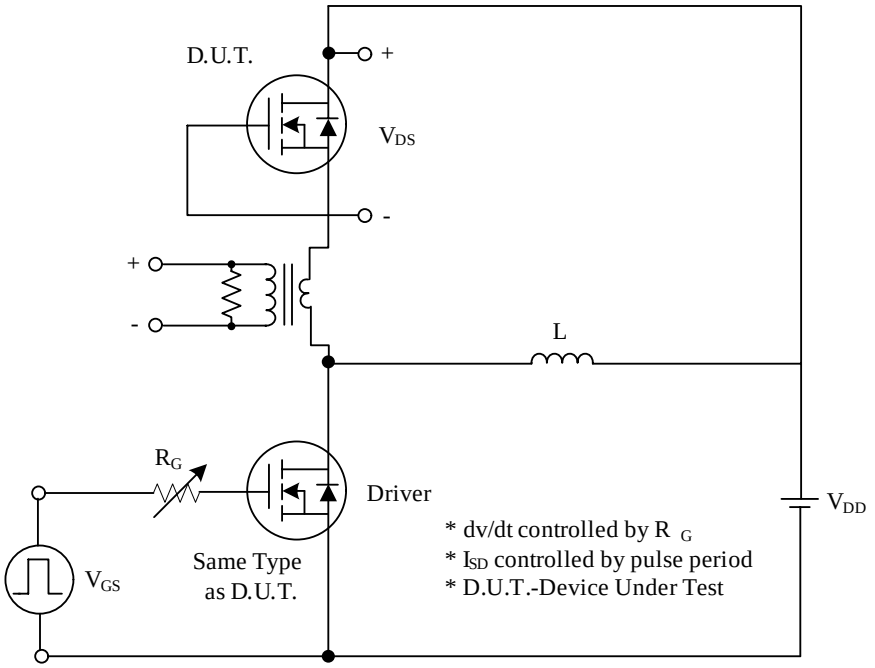


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

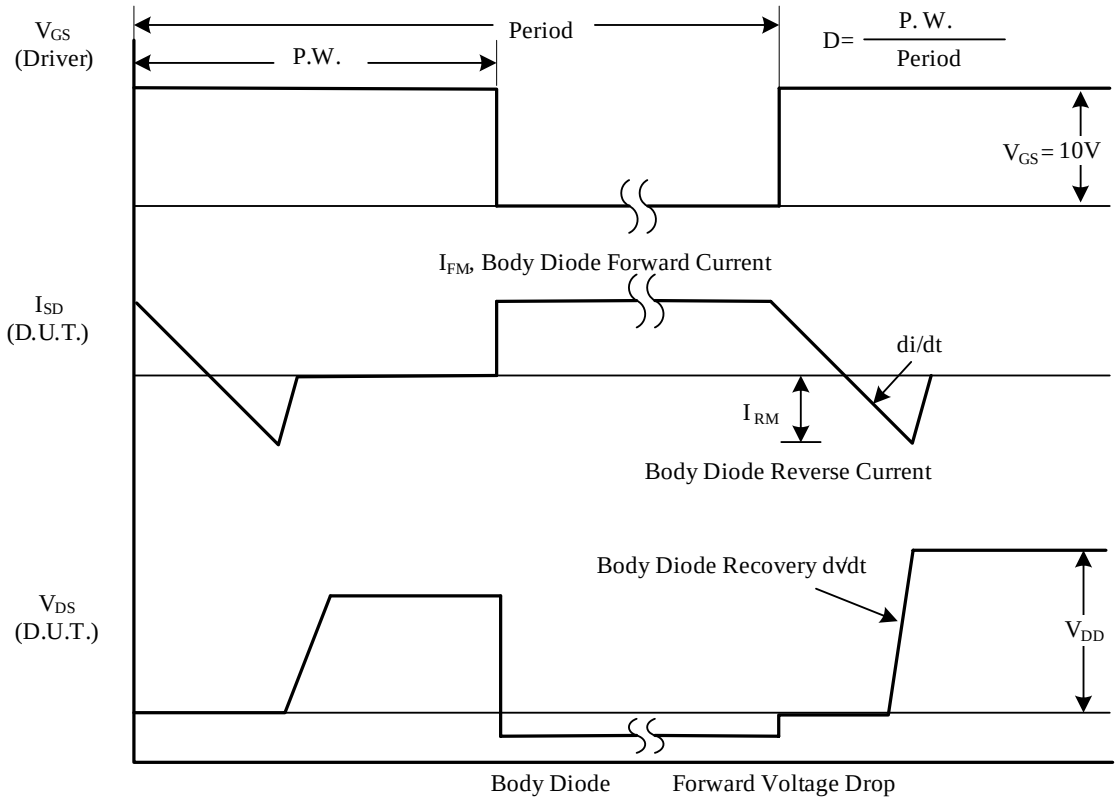


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

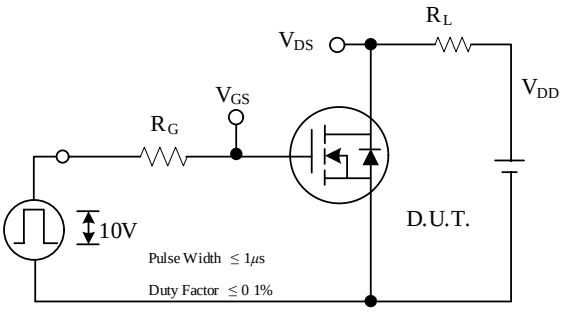


Fig. 2A Switching Test Circuit

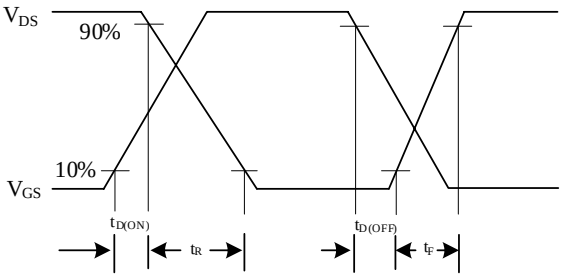


Fig. 2B Switching Waveforms

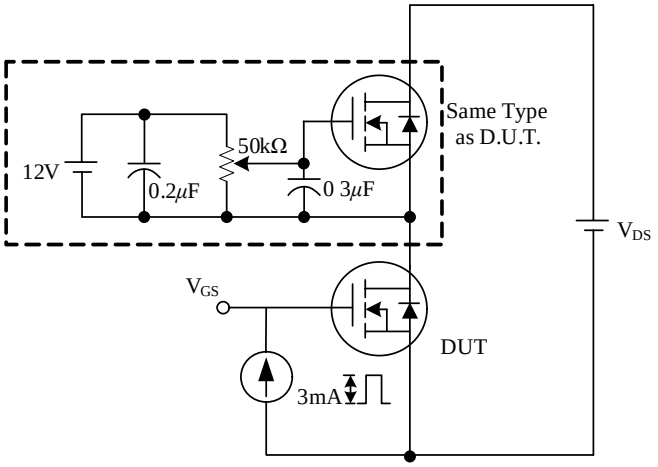


Fig. 3A Gate Charge Test Circuit

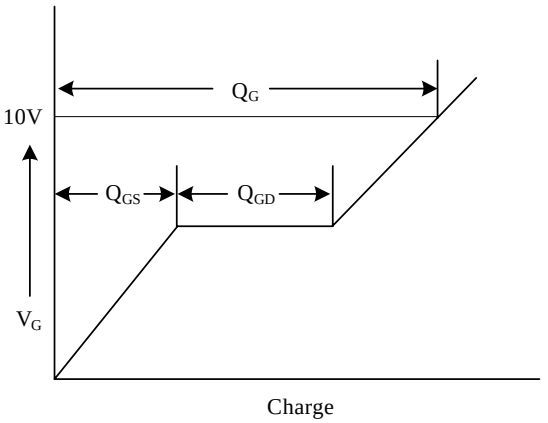


Fig. 3B Gate Charge Waveform

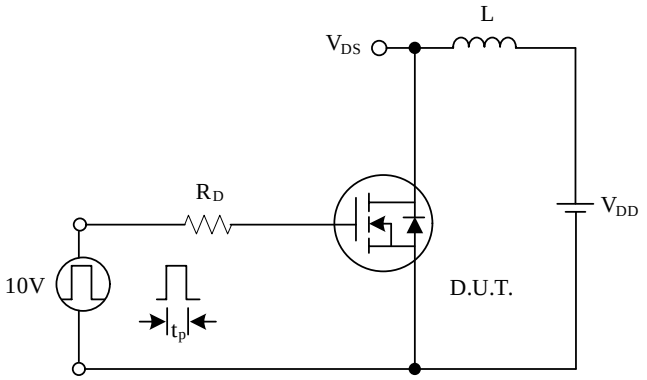


Fig. 4A Unclamped Inductive Switching Test Circuit

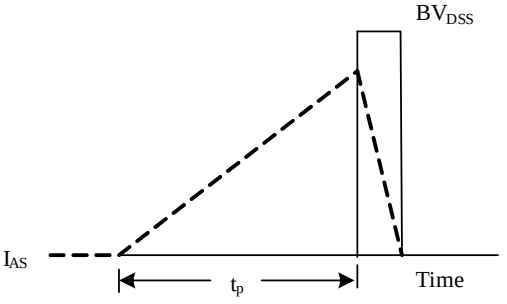


Fig. 4B Unclamped Inductive Switching Waveforms