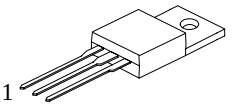
7Amps, 650Volts N-Channel Super Juction MOS-FET

Product Summary

V_{DS} @ $T_{j,max}$	650V
$R_{DS(on),max}$	0.64Ω
I_{DM}	28A
$Q_{g,typ}$	16nC

P :



TO-220

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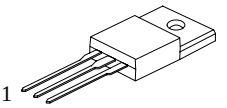

TO-220F

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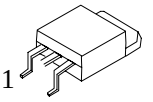

TO-252

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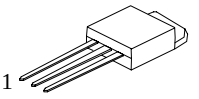

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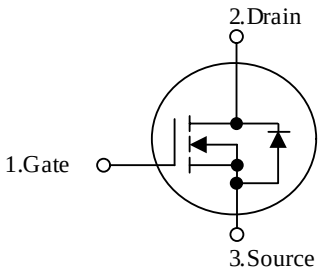
DESCRIPTION

FTK7NS65 Power MOS FET is fabricated using advanced super junction technology. The resulting device has extremely low on resistance, making it especially suitable for applications which require superior power density and outstanding efficiency.

FEATURES

- □ Ultra fast body diode
- □ Ultra low $R_{DS(on)}$
- □ Ultra low gate charge (typ. Q_g = 16nC)
- □ 100% UIS tested
- □ RoHS compliant

SYMBOL



Applications

- □ Power faction correction (PFC).
- □ Switched mode power supplies (SMPS).
- □ Uninterruptible power supply (UPS).

ORDERING INFORMATION

Order Number	Package	Pin Assignment			Packing
		1	2	3	
FTK7NS65P	TO-220	G	D	S	Tube
FTK7NS65F	TO-220F	G	D	S	Tube
FTK7NS65D	TO-252	G	D	S	Reel & Taping
FTK7NS65I	TO-251	G	D	S	Tube

Note: Pin Assignmen: G: Gate D: Drain S: Source

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DSS}	650	V
Continuous drain current (T_C = 25°C)	I_D	7	A
(T_C = 100°C)		4.4	A
Pulsed drain current [1]	I_{DM}	28	A
Gate - Source voltage	V_{GSS}	± 30	V
Avalanche energy, single pulse [2]	E_{AS}	261	mJ
Avalanche energy, repetitive [1]	E_{AR}	0.5	mJ
Avalanche current, repetitive [1]	I_{AR}	2	A
Power Dissipation (T_C = 25°C)	P_D	83	W
- Derate above 25°C		0.67	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C
Continuous diode forward current	I_S	7	A
Diode pulse current	$I_{S,pulse}$	28	A

Thermal CharacteristicsTO-220/TO-251/TO-252

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62	°C/W

Thermal Characteristics TO-220F

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4.3	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	80	°C/W

Electrical Characteristics

T_c = 25°C unless otherwise noted

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source on State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=3.5A	--	0.55	0.64	Ω
Gate resistance	R_g	f=1MHz	--	7.0	--	Ω
Input Capacitance	C_{iss}	V_{DS}=100V, V_{GS}=0V, f=1.0MHz	--	423	--	pF
Output Capacitance	C_{oss}		--	27	--	
Reverse Transfer Capacitance	C_{rss}		--	1.9	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=325V, I_D=7.0A, V_{GS}=10V, R_G=24Ω (Note 4,5)	--	16	--	ns
Turn-on Rise Time	t_r		--	29	--	
Turn-off Delay Time	$t_{d(off)}$		--	44	--	
Turn-off Fall Time	t_f		--	26	--	
Total Gate Charge	Q_g	V_{DS}=520V, I_D=7.0A, V_{GS}=10V (Note 4,5)	--	--	--	nC
Gate-Source Charge	Q_{gs}		--	3.6	--	
Gate-Drain Charge	Q_{gd}		--	8.3	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	7.0	A
Pulsed Source Current	I_{SM}		--	--	28	
Diode Forward Voltage	V_{SD}	I_S=7.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=7.0A,V_{GS}=0V, dI_F/dt=100A/μs (Note 4)	--	346	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.5	--	μC

Notes:

1. L=79mH,I_{AS}=2.4A,V_{DD}=100V, R_G=25Ω, starting temperature T_J=25°C;
2. V_{DS}=0~400V,I_{SD}<=7.0A, T_J=25°C;
3. V_{DS}=0~480V;
4. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
5. Essentially independent of operating temperature.

Typical Characteristics

Figure 1. On-Region Characteristics

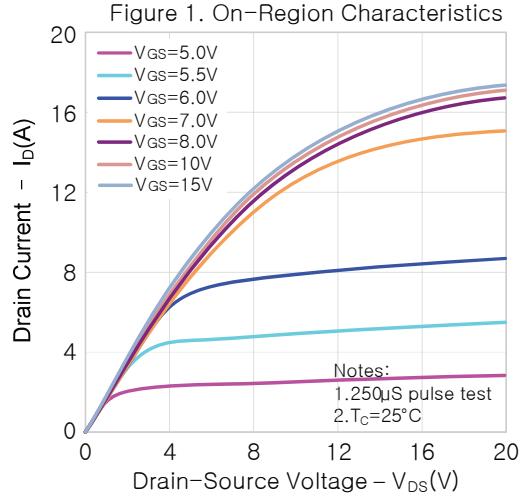


Figure 2. Transfer Characteristics

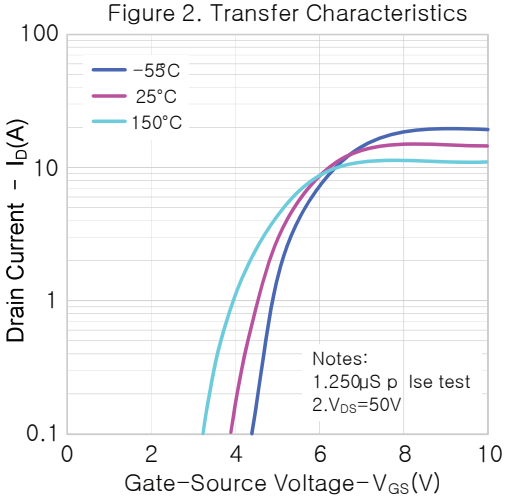


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

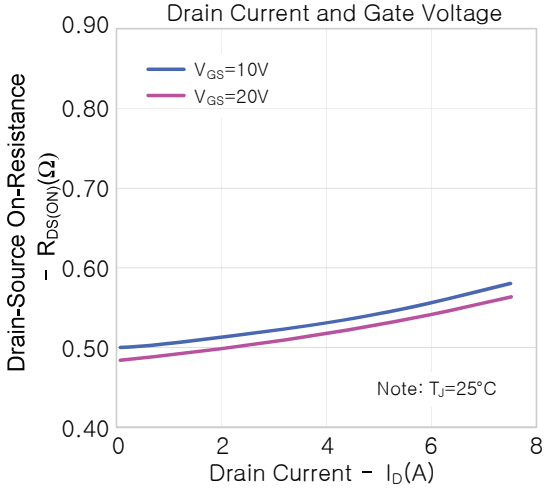


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

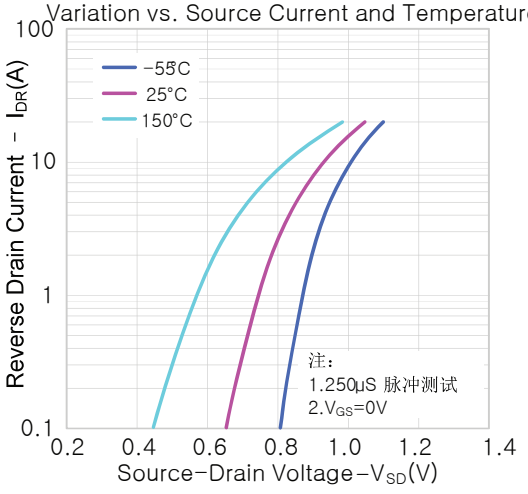


Figure 5. Capacitance Characteristics

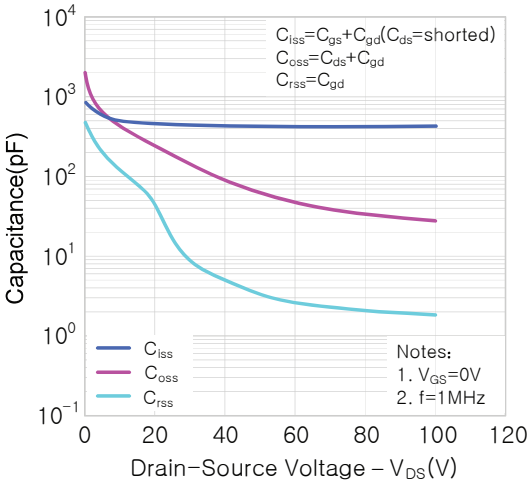


Figure 6. Gate Charge Characteristics

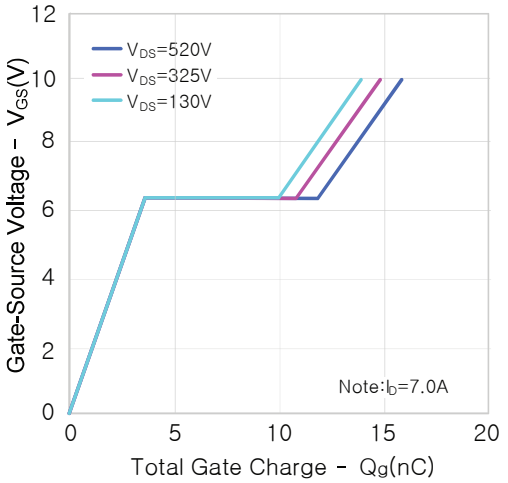


Figure 7. Breakdown Voltage Variation vs. Temperature

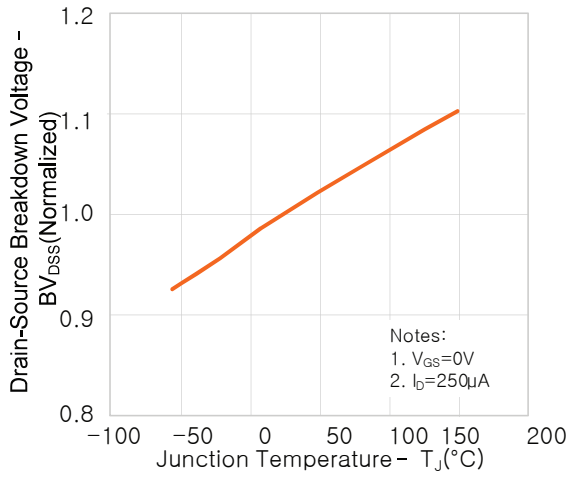


Figure 8. On-resistance Variation vs. Temperature

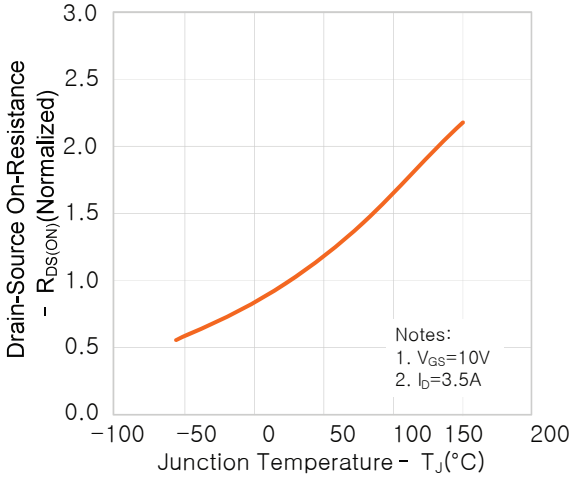


Figure 9-1. Max. Safe Operating Area (FTK7N65DD2/MJD2)

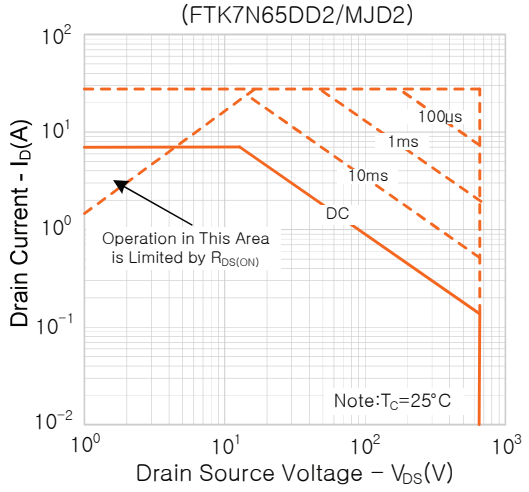
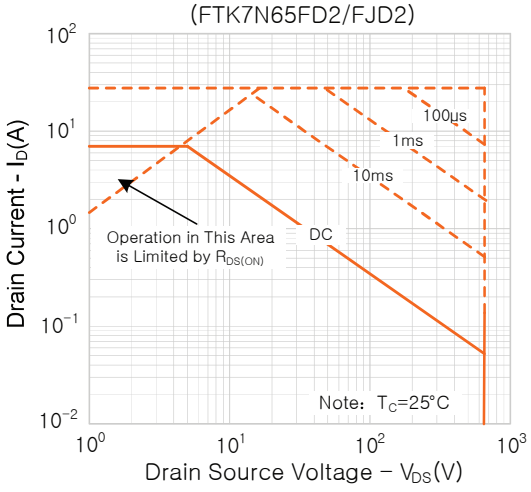


Figure 9-2. Max.Safe Operating Area (FTK7N65FD2/FJD2)



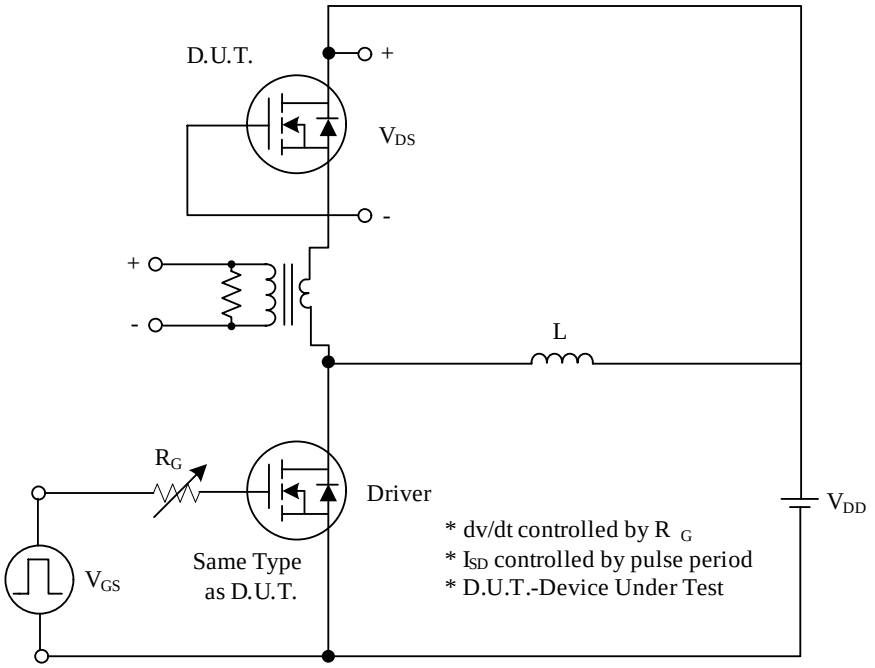


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

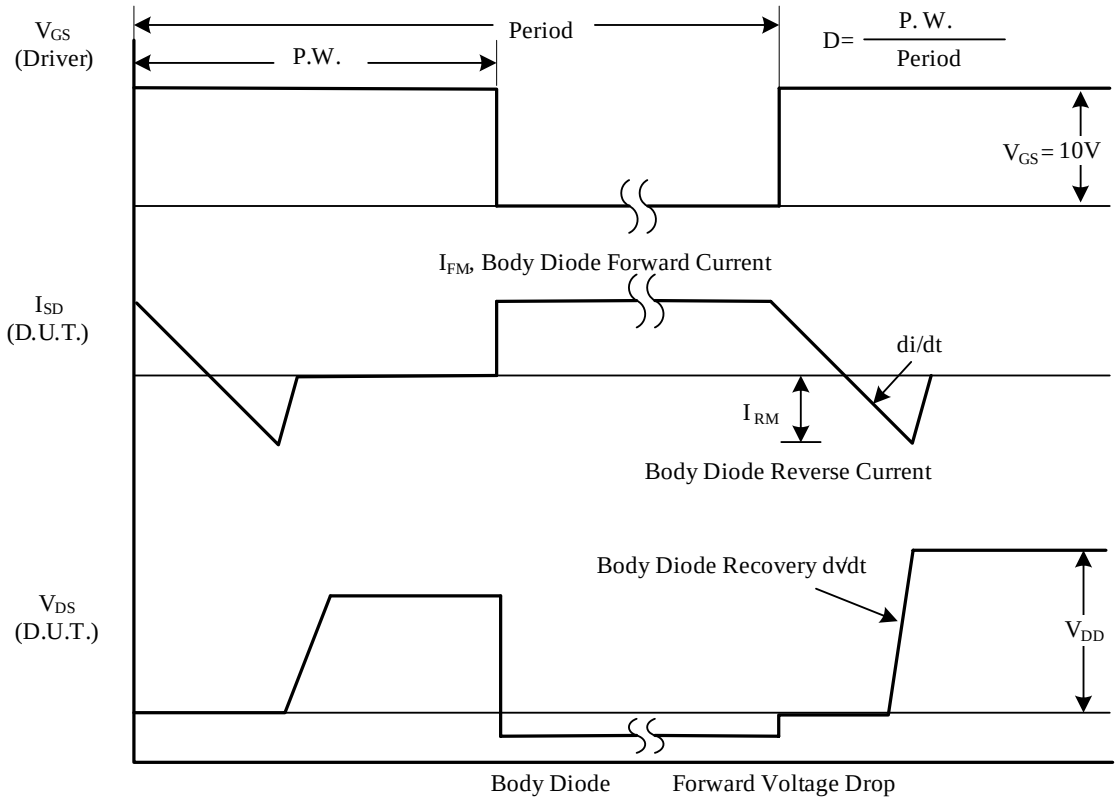


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

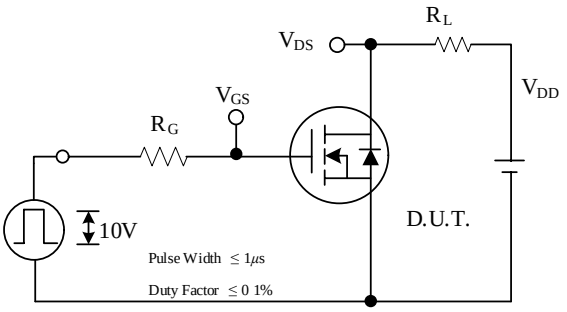


Fig. 2A Switching Test Circuit

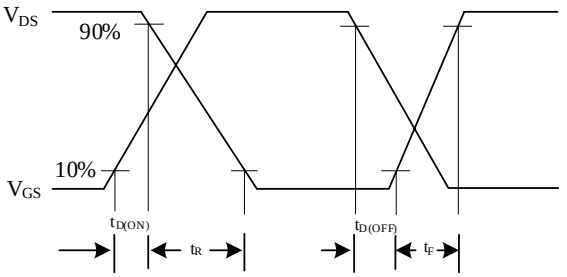


Fig. 2B Switching Waveforms

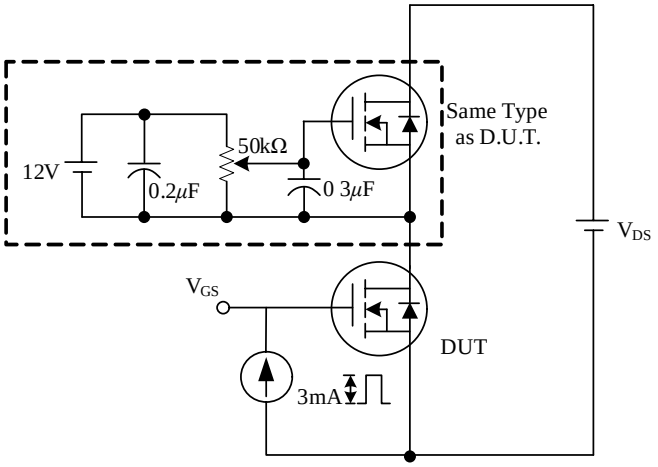


Fig. 3A Gate Charge Test Circuit

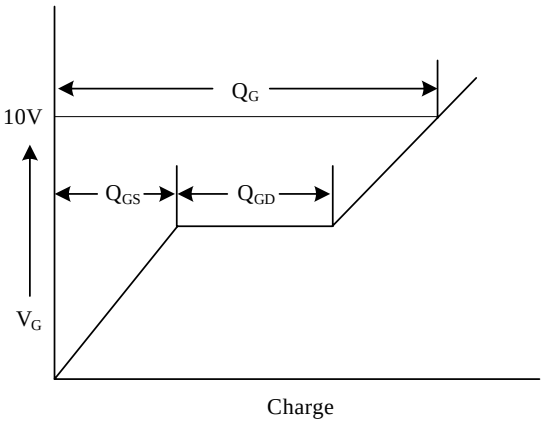


Fig. 3B Gate Charge Waveform

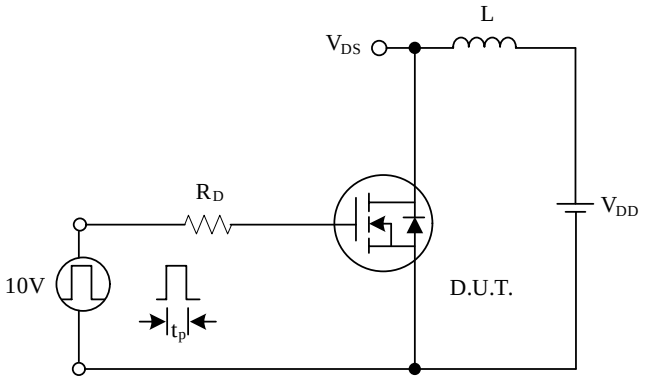


Fig. 4A Unclamped Inductive Switching Test Circuit

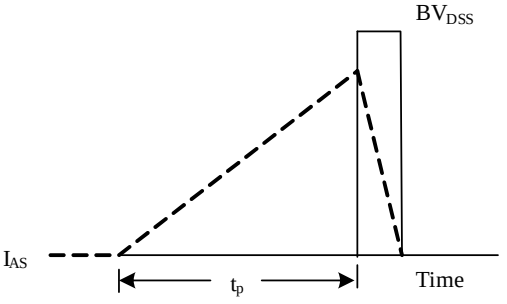


Fig. 4B Unclamped Inductive Switching Waveforms