12V, 4.0 mΩ, 8.5A, Dual N-Channel

Vsss	Rss(on) Max	I_D
12V	4.0 mΩ@4.5V	8.5A
	4.3 mΩ@3.8V	
	4.9 mΩ@4.1V	
	6.8 mΩ@2.5V	

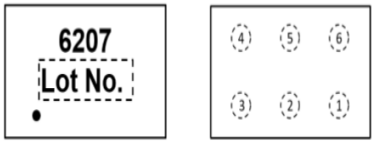
Feature

- Rss(on) Max = 5.0mΩ(VGS=4.5V)
- 2KV ESD HBM
- Common-Drain Type
- ESD Protected Gate
- Pb-Free, Halogen-Free & RoHS Compliance

Application

- Lithium Ion Battery

Marking and pin assignment

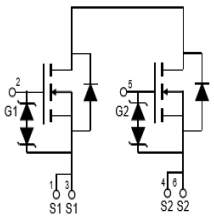


Top View Bottom View

1,3. Source1 2. Gate1

4,6. Source2 5. Gate2

Equivalent Circuit



Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Maximum	Units
Source to Source Voltage	V_{SSS}	12	V
Gate to Source Voltage	V_{GSS}	±8	V
Source Current(DC)	I_S	8.5	A
Source Current(Pulse) PW≤10μs, Duty Cycle≤1%	I_{SP}	85	A
Total Dissipation(Note2)	P_T	2.1	W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{stg}	-55 ~ 150	℃

Note 1: Stresses exceeding those listed In the maximum ratings table may damage the device If any of those limits are exceeded , device functionality should not be assumed. Damage may occur and reliability may be affected

Thermal Resistance Ratings

Parameter	Symbol	Value	Units
Thermal Resistance(j-a)	$R_{\Theta JA}$	75	℃/W

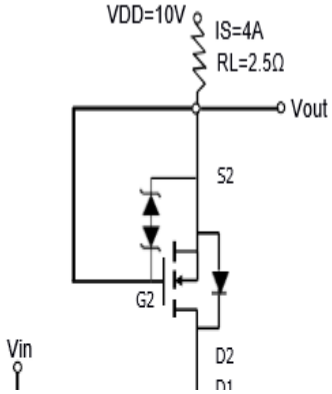
Note2 : Surface mounted on ceramic substrate(5000 ㎟ × 0.8㎜)

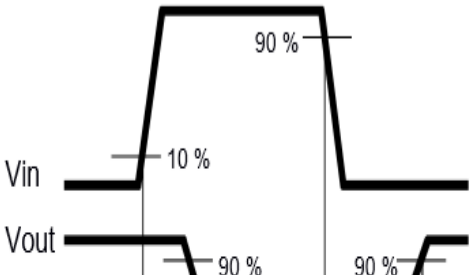
Electrical Characteristics (25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source to Source Breakdown Voltage	$V_{(BR)SSS}$	IS = 1 mA, VGS = 0 V (Test Circuit 1)	12			V
Zero Gate Voltage Source Current	I_{SSS}	VGS = 10V, VSS = 0 V (Test Circuit 1)			1	μA
Gate To Source Leakage Current	I_{GSS}	VGS = ±8V, VSS = 0 V (Test Circuit 2)			±10	μA
Gate Threshold Voltage	$V_{(GS)th}$	IS = 250μA, VSS =10V (Test Circuit 3)	0.4	0.95	1.4	V
Static Source to Source On-State Resistance	$R_{SS(on)}$	IS = 4.0 A, VGS = 4.5 V (Test Circuit 4)	2.6	4.0	5.0	mΩ
		IS = 4.0 A, VGS = 3.8 V (Test Circuit 4)	2.8	4.3	5.5	
		IS = 4.0 A, VGS = 3.1 V (Test Circuit 4)	3.2	4.9	6.5	
		IS = 4.0 A, VGS = 2.5 V (Test Circuit 4)	3.8	6.8	10.5	
Turn On Delay Time	$td_{(on)}$	VSS = 10 V, VGS = 4.0V ,RL = 2.5Ω (Test Circuit 5)		0.5		μs
Rise Time	tr			1.3		
Turn-Off Delay Time	$td_{(OFF)}$			3.3		
Fall Time	tf			3.2		
Total Gate Charge	Qg	VSS = 10 V VGS =8 V, IS = 4.0 A (Test Circuit 6)		32		nC
Forward Source to Source Voltage	$V_{F(S-S)}$	IF = 6.0 A, VGS = 0 V (Test Circuit 7)			1.5	V

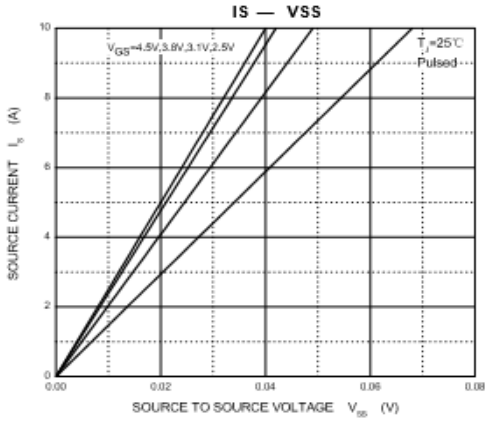
Note3 : Product parametric performance is indicated in the electrical characteristics for the listed test condition , unless otherwise noted product performance may not be indicated by the electrical characteristics if operated under different condition

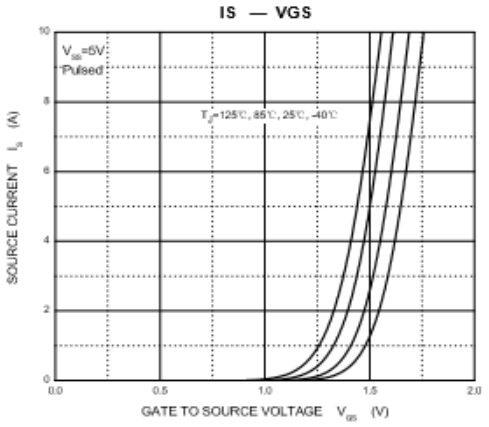
Notes:
1.Mounted onFR4 board(25.4mm 25.4mm t1.0mm) using the minimum recommended pad size(36um Copper).
2.t= 10us , DutyCycle≤1 %. 3.Measurement circuitfor td(on)/tr/td(off)/tf,whenFET1is measured,G2and S2are short-circuited.

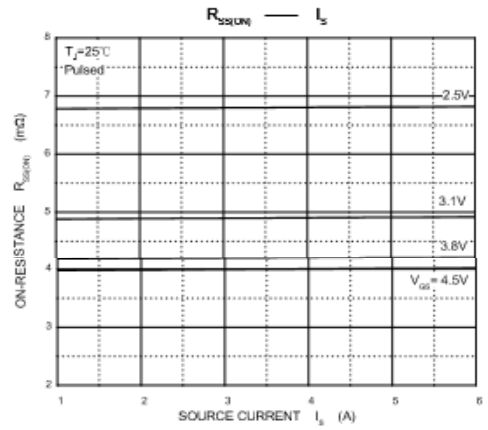


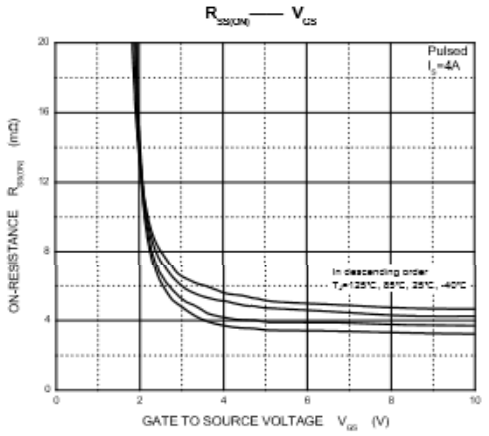


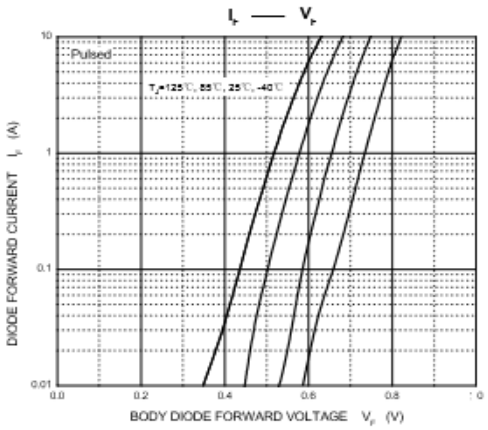
Typical Characteristics

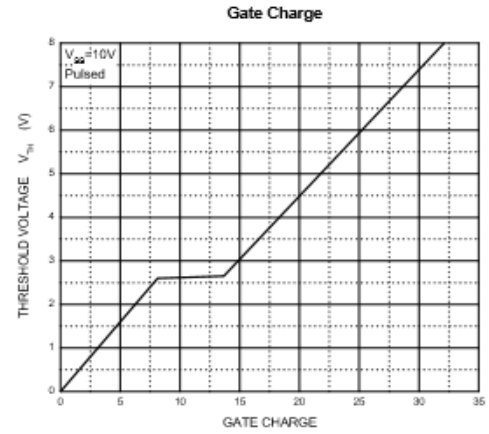




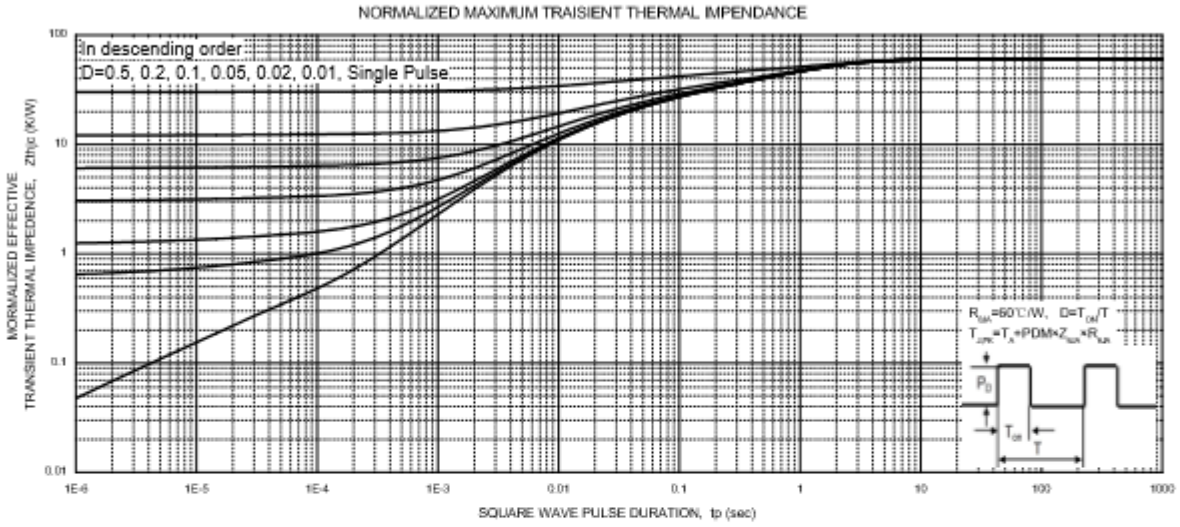


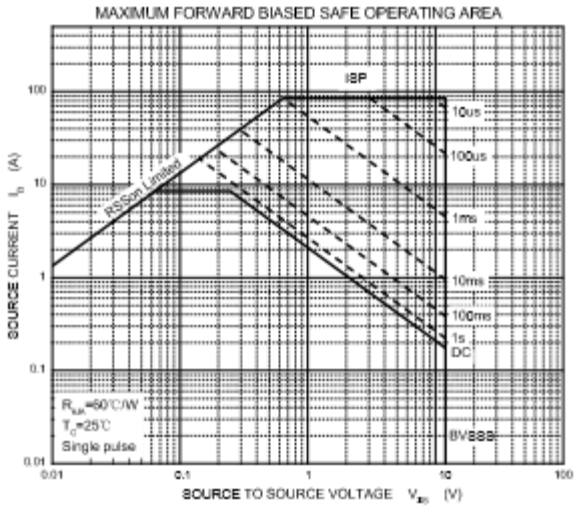




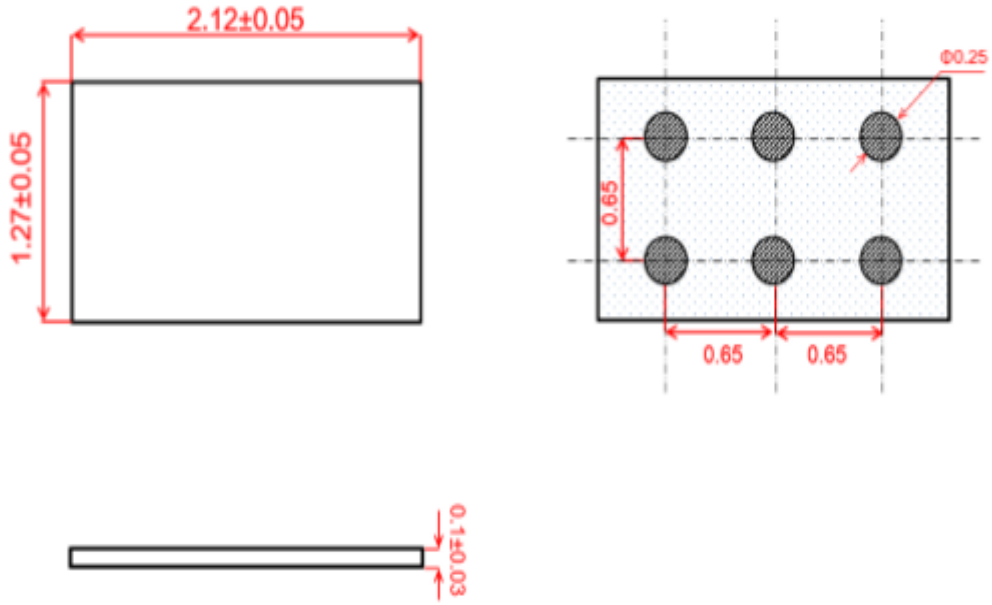


Typical Characteristics

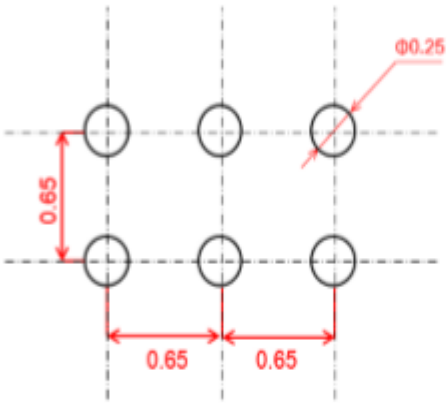




Package Outline Dimensions(Unit:mm)



Suggested Pad Layout (Unit:mm)



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.