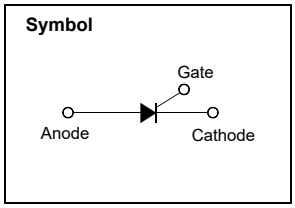
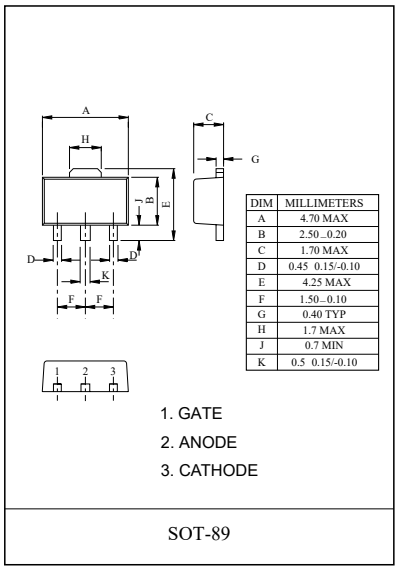
Silicon Planar PNPN Thyristor

DESCRIPTION

Logic level sensitive gate triac intended
to be interfaced directly to microcontrollers,
logic integrated circuits
and other low power gate trigger circuits.





FEATURES

- Blocking voltage to 400 V (MCR100-6/F) , 600V (MCR100-8/F)
- RMS on-state current to 0.8 A
- General purpose switching

APPLICATIONS

- General purpose switching
- Phase control applications
- Solid state relays.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Storage junction temperature range	T_{stg}	-55-150	℃
Operating junction temperature range	T_j	-40-125	℃
Repetitive peak off-state voltage	V_{DRM}	600	V
Repetitive peak reverse voltage	V_{RRM}	600	V
RMS on-state current	$I_{T(RMS)}$	0.8	A
Non repetitive surge peak on-state current (tp=10ms)	I_{TSM}	12	A
I^2t value for fusing (tp=10ms)	I^2t	0.72	A^2S
Critical rate of rise of on-state current	dI/dt	50	A/μS
Peak gate current (tp=20μS,Tj=110℃)	I_{GM}	0.3	A
Peak gate power (tp=20μS,Tj=110℃)	P_{GM}	0.5	W
Average gate power dissipation (Tj=110℃)	$P_{G(AV)}$	0.1	W

ELECTRICAL CHARACTERISTICS (Tamb=25℃ unless otherwise specified)

Parameter	Symbol		Test conditions	MIN	MAX	UNIT
On state voltage *	V_{TM}		I_{TM}=1A		1.7	V
Gate trigger voltage	V_{GT}		V_{AK}=7V		0.8	V
Peak Repetitive forward and reverse blocking voltage MCR100-6/F	V_{DRM} AND V_{RRM}		I_{DRM}= 10 μA	400		V
MCR100-8/F				600		
Peak forward or reverse blocking current	I_{DRM} I_{RRM}		V_{AK}= Rated V_{DRM} or V_{RRM}		10	μA
Holding current	I_H		I_{HL}=20mA ,V_{AK} =7V		5	mA
Gate trigger current	I_{GT}	B	V_{AK}=7V	30	80	μA

* Forward current applied for 1 ms maximum duration，duty cycle≤1%。

Symbol	Test Condition	Value			Unit
		MIN.	TYP.	MAX.	
dV/dt	V_D=2/3V_{DRM} T_J=110℃ R_{GK}=1KΩ	100	200	-	V/μs

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	junction to case	38	℃/W

Typical Characteristics

FIGURE 1 – MCR100-8 CURRENT DERATING
(REFERENCE: CASE TEMPERATURE)

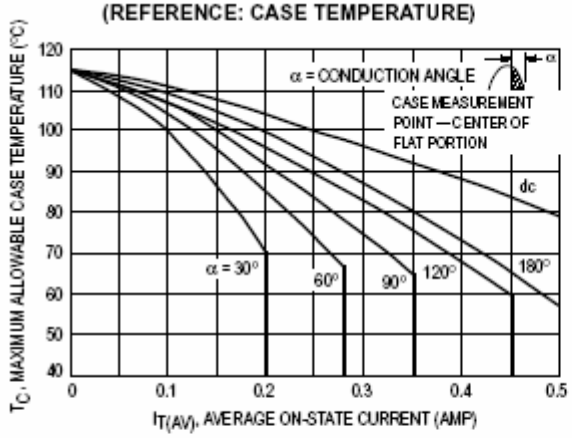


FIGURE 2 – MCR100-8 CURRENT DERATING
(REFERENCE: AMBIENT TEMPERATURE)

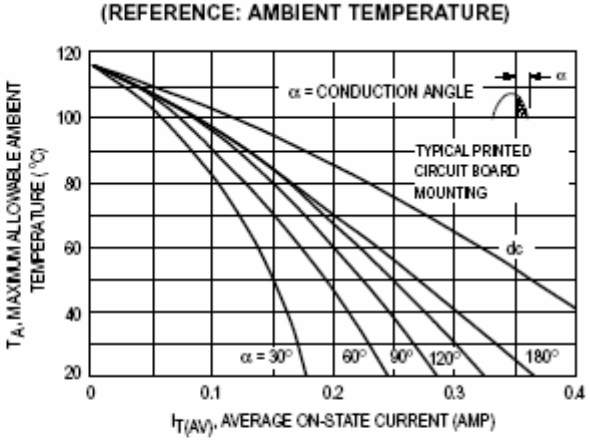


FIGURE 3: Maximum power dissipation versus RMS on-state current

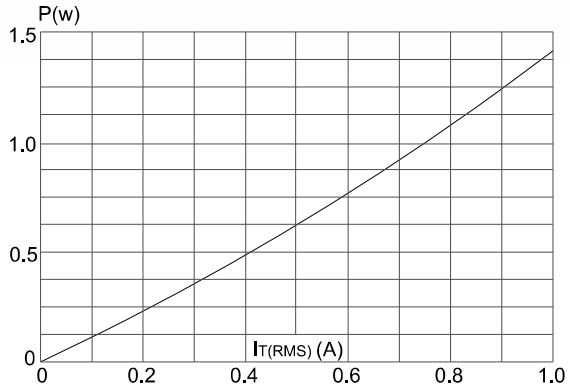


FIGURE 4: RMS on-state current versus case temperature

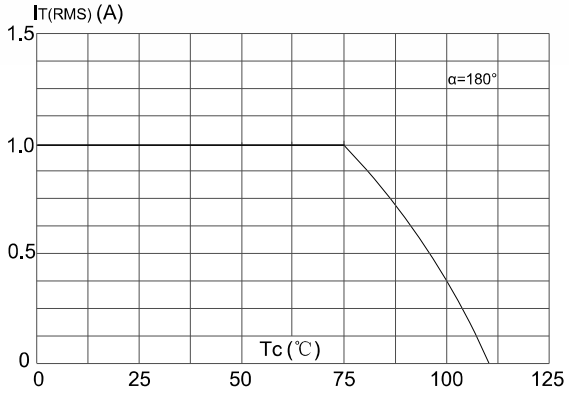


FIGURE 5 : Surge peak on-state current versus number of cycles

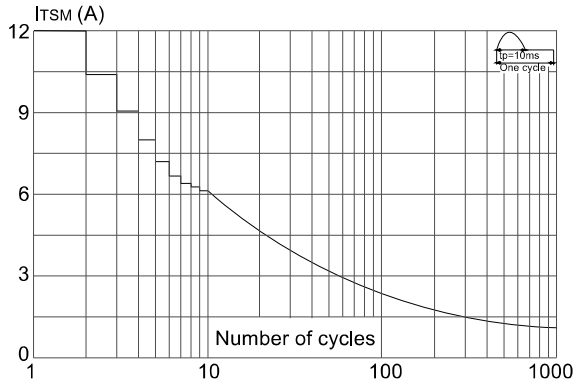


FIGURE 6: On-state characteristics (maximum values)

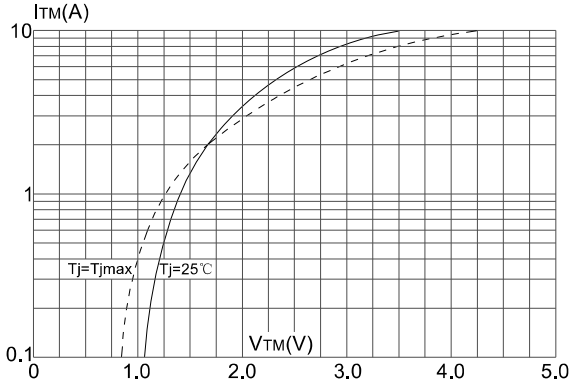


FIGURE 7 : Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<10ms (dI/dt ≤ 50A/μs)

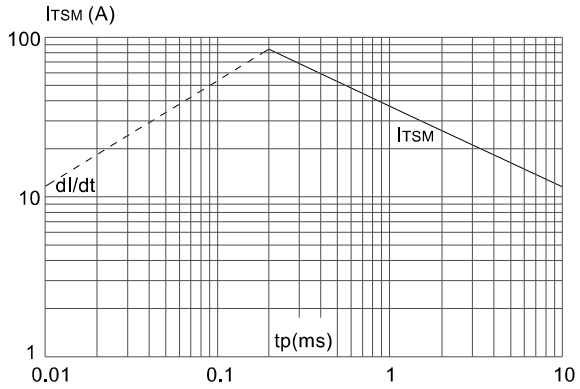


FIGURE 8 : Relative variations of gate trigger current, holding current and latching current versus junction temperature