

BT136-600 TRIAC

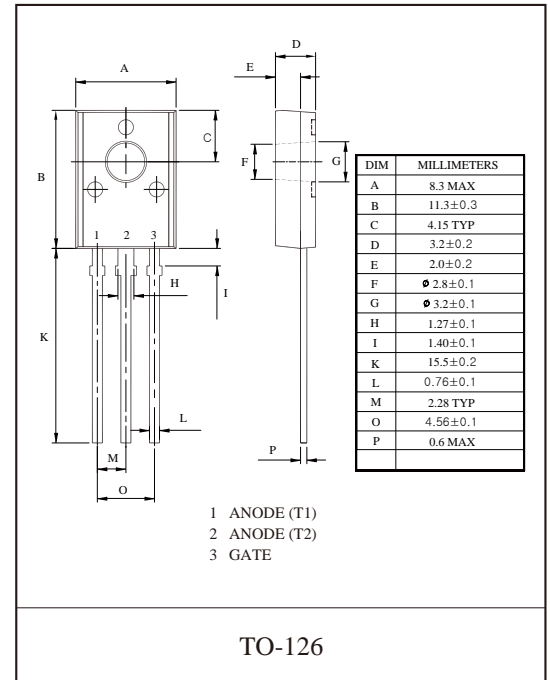
MAIN FEATURES

Symbol	value	unit
$I_{T(RMS)}$	4	A
V_{DRM}/V_{RRM}	600	V
I_{TSM}	25	A

GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope , intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance.

Typical applications include motor control, industrial and domestic lighting , heating and static switching.



ABSOLUTE MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

symbol	parameter	value	unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	$T_C=107^\circ C$	4 A
I_{TSM}	Non repetitive surge peak on-state current (full sine wave, $T_j=25^\circ C$)	$t=20ms$	25 A
		$t=16.7ms$	27 A
I_{GM}	Peak gate current		2 A
$P_{G(AV)}$	Average gate power dissipation	$T_j=125^\circ C$	0.5 W
T_{stg}	Storage junction temperature range		-40 to +150 °C
T_j	Operating junction temperature range		-40 to +125 °C

ELECTRICAL CHARACTERISTICS (Ta=25°C unless otherwise specified)

Parameter	Symbol	Test conditions	Min	Max	Unit
Rated repetitive peak off-state/reverse voltage	V_{DRM}, V_{RRM}	$I_D=10\mu A$	600		V
Rated repetitive peak off-state current	I_{DRM}, I_{RRM}	$V_D=620V$		10	μA
On-state voltage	V_{TM}	$I_T=5A$		1.7	V
Gate trigger current	I_{GT}	$V_D=12V$ $R_L=100\Omega$	I	5	mA
			II	5	mA
			III	5	mA
			IV	10	mA
Gate trigger voltage	V_{GT}	$V_D=12V$ $R_L=100\Omega$	I	1.45	V
			II	1.45	V
			III	1.45	V
			IV	1.7	V
Holding current	I_H	$I_T=100mA$ $I_G=20mA$		10	mA

■ Performance Curves

Fig 1. Gate Characteristics

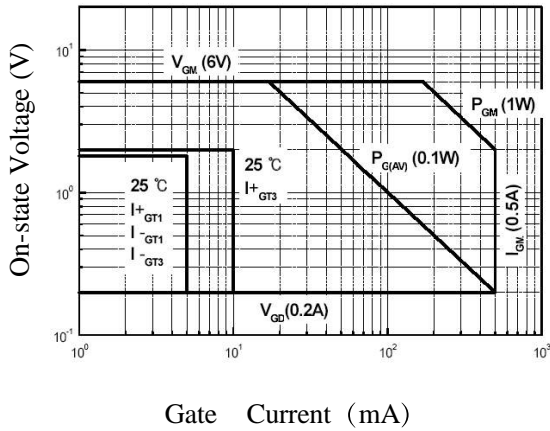


Fig 2. On-State Voltage

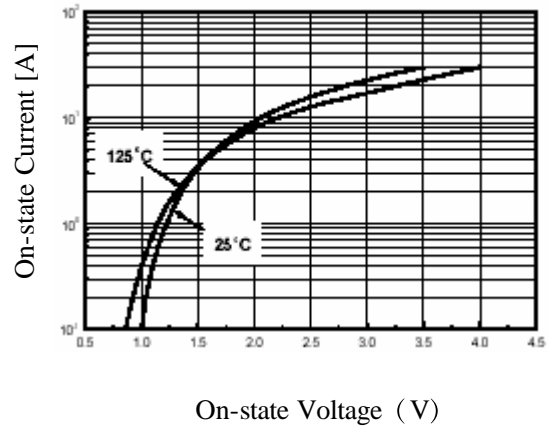


Fig 3. Gate Trigger Voltage vs. Junction Temperature

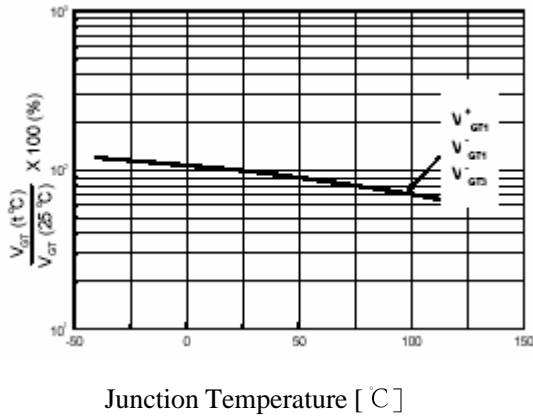


Fig 4. On State Current vs. Maximum Power Dissipation

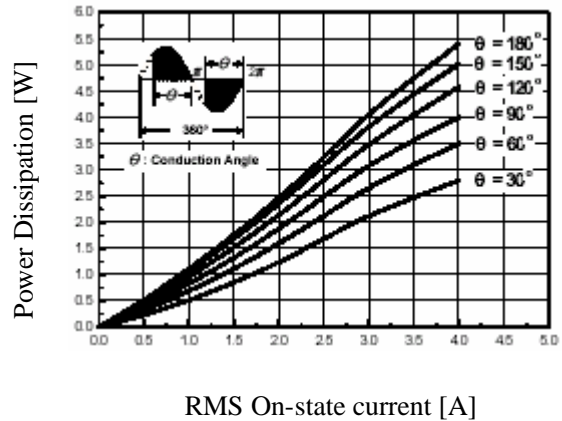


Fig 5. On State Current vs. Allowable Case Temperature

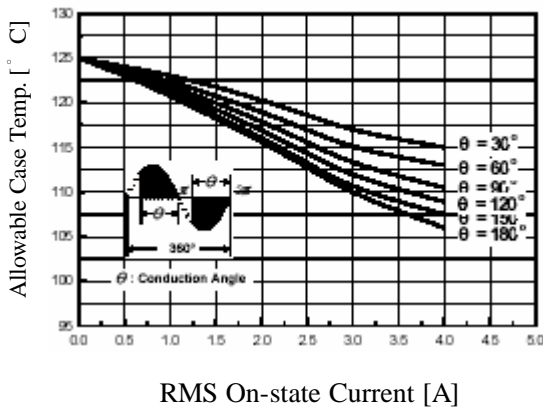


Fig 6. Surge On-State Current Rating (Non-Repetitive)

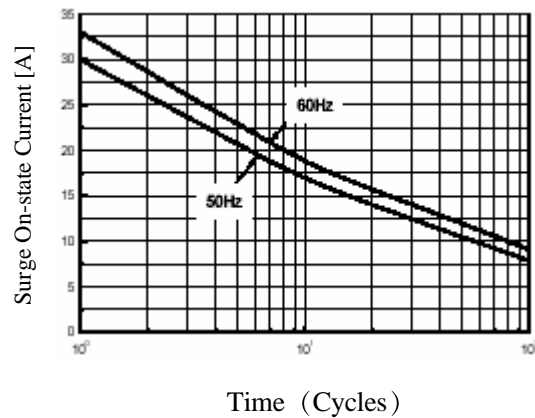


Fig 7. Gate Trigger Current vs. Junction Temperature

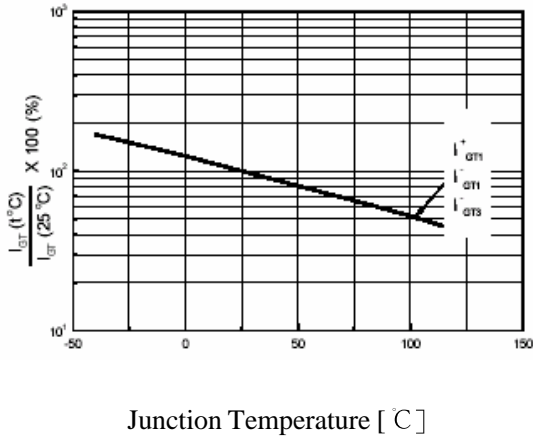


Fig 8. Transient Thermal Impedance

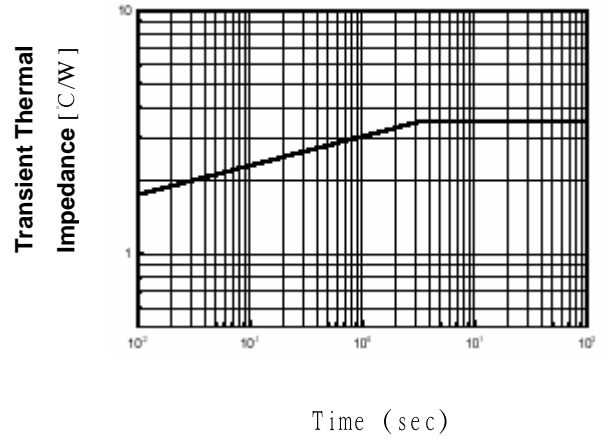
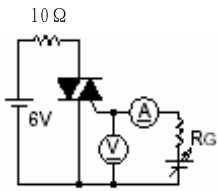
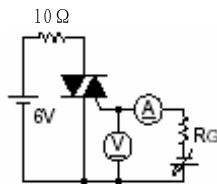


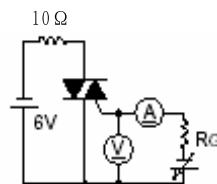
Fig 9. Gate Trigger Characteristics Test Circuit



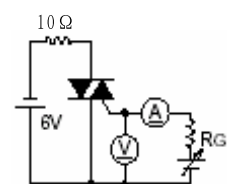
Test Procedure I



Test Procedure II



Test Procedure III



Test Procedure IV