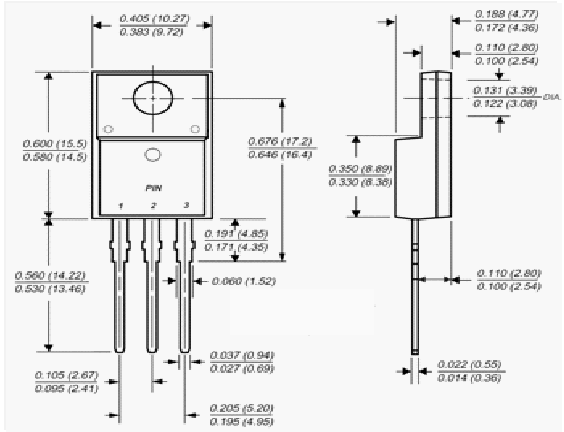
Bi-Directional Triode Thyristor

Designed for high performance full-wave ac control applications where high noise immunity and high commutating di/dt are required.

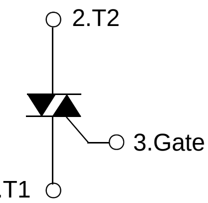
TO-220F



Features

- Blocking Voltage to 800 V
- On-State Current Rating of 12A RMS at 80℃
- Uniform Gate Trigger Currents in Three Quadrants
- High Immunity to dV/dt-1500V/us minimum at 125℃
- Minimizes Snubber Networks for Protection
- Industry Standard TO-220F Package
- High Commutating dI/dt- 4.0A/ms minimum at 125℃
- Internally Isolated (2500VRMS)
- These are Pb-Free Devices

Symbol



Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current(full since wave)	TO-220F	TC=85℃	12	A
I_{TSM}	Non repetitive surge peak on-state current(full cycle, Tj initial=25℃)	F=50Hz	t=20ms	120	A
		F=60Hz	t=16.7ms	126	
I^2t	I^2t Value for fusing	tp=10ms		78	A^2s
DI/DT	Critical rate of rise of on-state current $IG=2X_{IGT,tr\le100ns}$	F=120Hz	Tj=125℃	50	A/us
VDSM/VRSM	Non repetitive surge peak off-state voltage	tp=10ms	Tj=25℃	Vdrm / vrrm + 100V	V
IGM	Peak gate current	tp=20us	Tj=125℃	4	A
$P_{G(AV)}$	Average gate power dissipation		Tj=125℃	1	W
T_{stg}	Storage junction temperature range			-40 to +150	℃
T_j	Operating junction temperature range			-40 to +125	

Electrical Characteristics (Tj=25℃,unless otherwise specified)

Snubberless™ and Logic Level(3 quadrants)

Symbol	Test conditions	Quadrant	BT12F-600B		Unit
I_{GT}(1)	V_D=12V R_L=33Ω	Ⅰ-Ⅱ-Ⅲ	MAX	50	mA
V_{GT}		Ⅰ-Ⅱ-Ⅲ	MAX	1.3	V
V_{GD}	V_D=V_{DRM} R_L=3.3KΩTj=125℃	Ⅰ-Ⅱ-Ⅲ	MIN	0.2	V
IH(2)	IT=100mA		MAX	50	mA
IL	I_G=1.2I_{GT}	Ⅰ-Ⅲ	MAX	70	mA
		Ⅱ		80	
Dv / Dt(2)	VD=67%V_{DRM} Gate open Tj=125℃		MIN	1000	V/us
(DI/dt)c(2)	(Dv/dt)c=0.1 V/us Tj=125℃		MIN	-	A/ms
	(Dv/dt)c=10V/us Tj=125℃			-	
	Without snubber Tj=125℃			12	

Standard (4 Quadrants)

Symbol	Test conditions	Quadrant	BT12F-600B		Unit
IGT(1)	VD=12V RL=33Ω	Ⅰ-Ⅱ-Ⅲ	MAX	50	mA
		Ⅳ		100	
VGT		ALL	MAX	1.3	V
VGD	VD=VDRM RL=3.3KΩTj=125℃	ALL	MIN	0.2	V
IH(2)	IT=500mA		MAX	50	mA
IL	IG=1.2IGT	Ⅰ-Ⅲ- Ⅳ	MAX	60	mA
		Ⅱ		120	
(DI/dt)(2)	VD=67%VDRM Gate open Tj=125℃		MIN	400	V/us
(DI/dt)c(2)	(Dv/dt)c=7 A/ms Tj=125℃		MIN	10	V/us

Static Characteristics

Symbol	Test conditions			Value	Unit
VTM(2)	ITM=11A tp=380us	TJ=25℃	MAX	1.55	V
Vto(2)	Threshold voltage	TJ=125℃	MAX	0.85	V
Rd(2)	Dynamic resistance	TJ=125℃	MAX	35	mΩ
I_{DRM} I_{RRM}	V_{DRM}=V_{RRM}	TJ=25℃	MAX	5	uA
		TJ=125℃		2	mA
V_{DRM}/V_{RRM}	Voltage	TJ=25℃	MIN	600 and 800	V

Note 1: minimum IGT is guaranted at 5% of IGT max

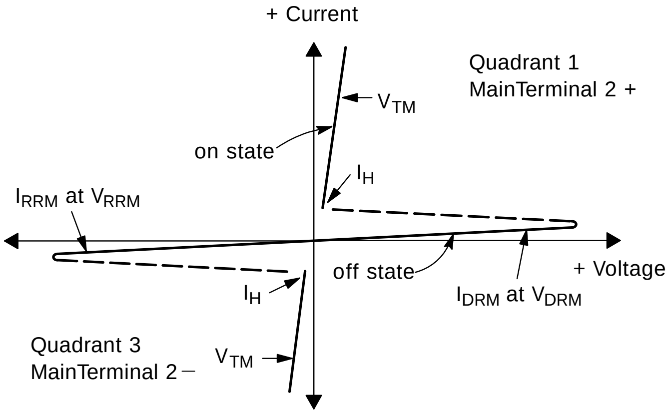
Note 2: for both polarities of A2 referenced to A1

Thermal Resistances

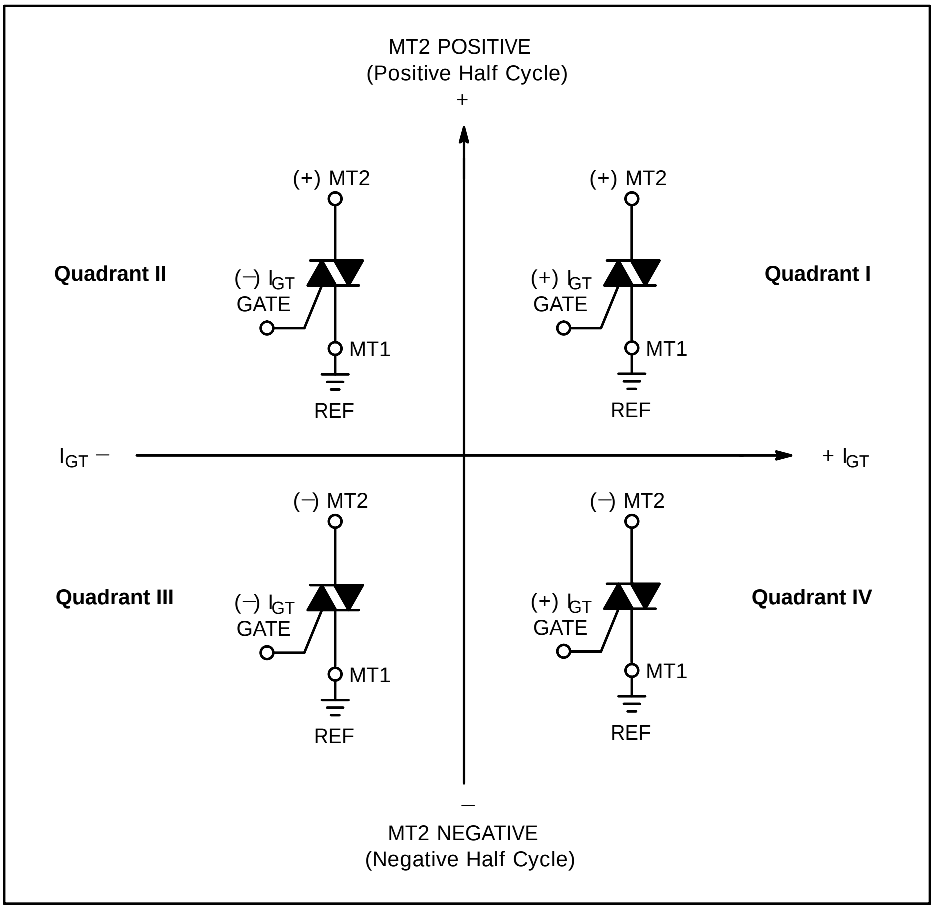
Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case(AC)	TO-220F	2.3	℃/W
Rth(j-a)	Junction to ambient	TO-220F	60	℃/W

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in–phase signals (using standard AC lines) quadrants I and III are used.

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

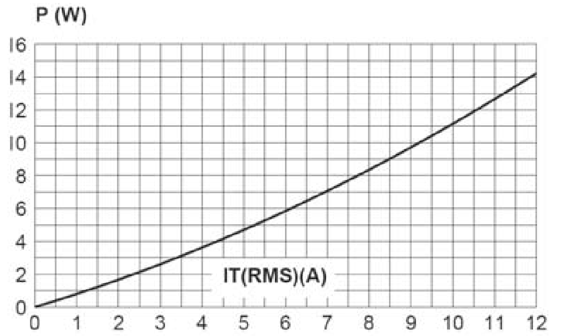


Fig. 2-1: RMS on-state current versus case temperature (full cycle).

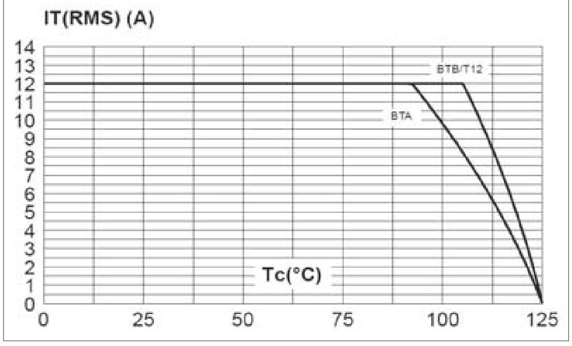


Fig. 2-2: RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35μm),full cycle.

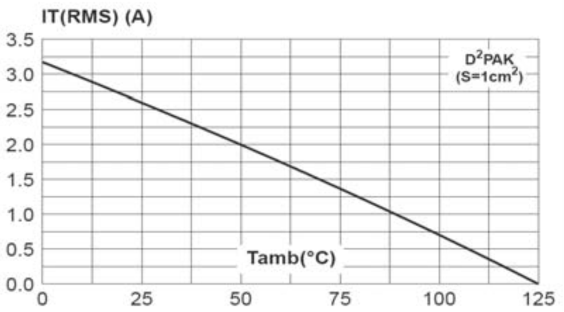


Fig. 3: Relative variation of thermal impedance versus pulse duration.

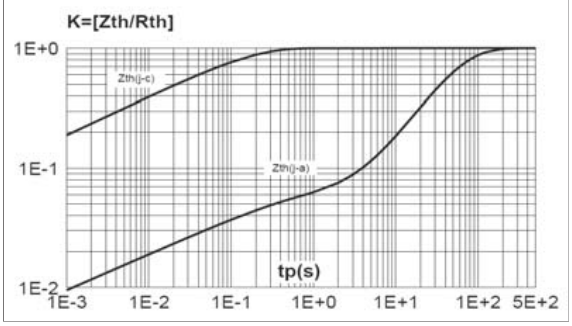


Fig. 4: On-state characteristics (maximum values).

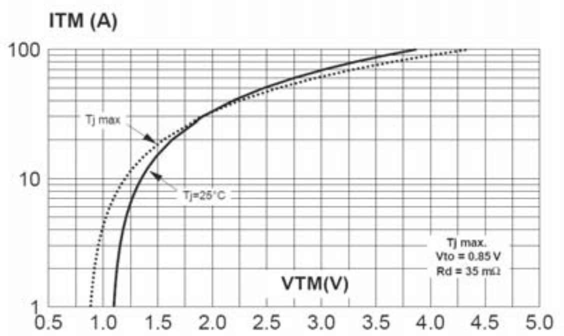


Fig. 5: Surge peak on-state current versus number of cycles.

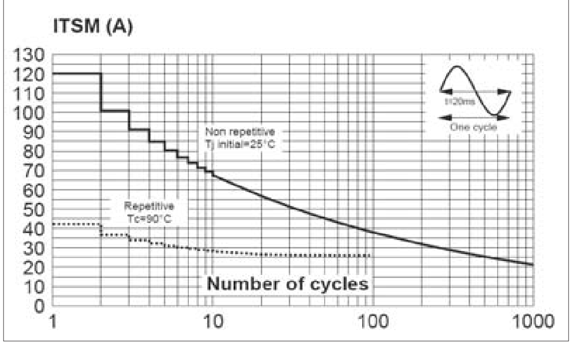


Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10ms, and corresponding value of I²t.

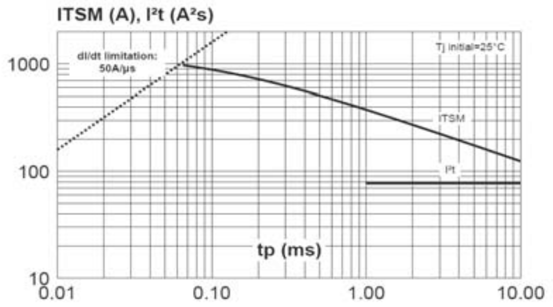


Fig. 7: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).

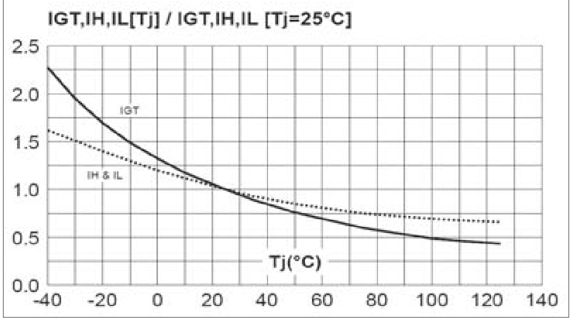


Fig. 8-1: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values) (BW/CW/T1235).

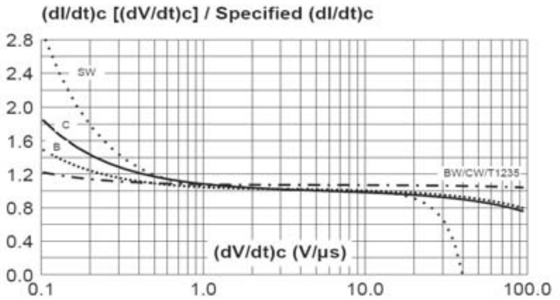


Fig. 8-2: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values) (TW).

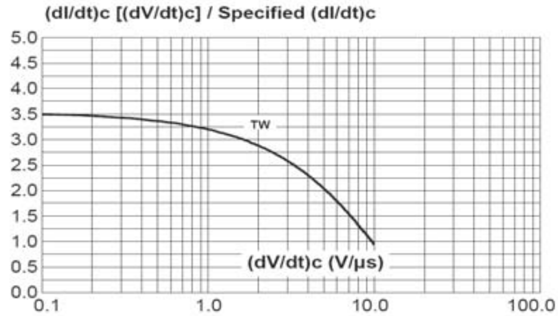


Fig. 9: Relative variation of critical rate of decrease of main current versus junction temperature.

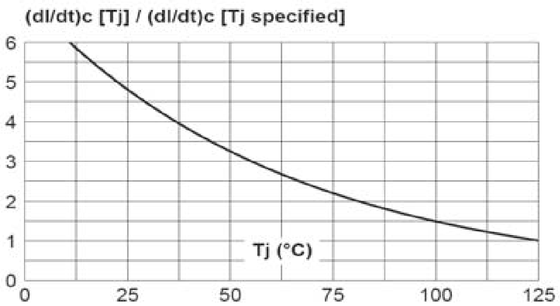


Fig. 10: D²PAK Thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35 µm).