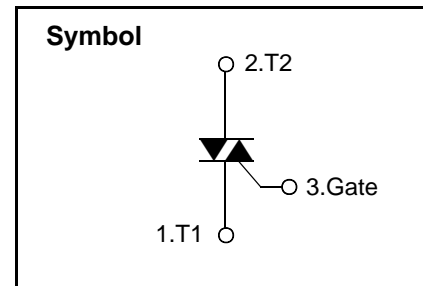
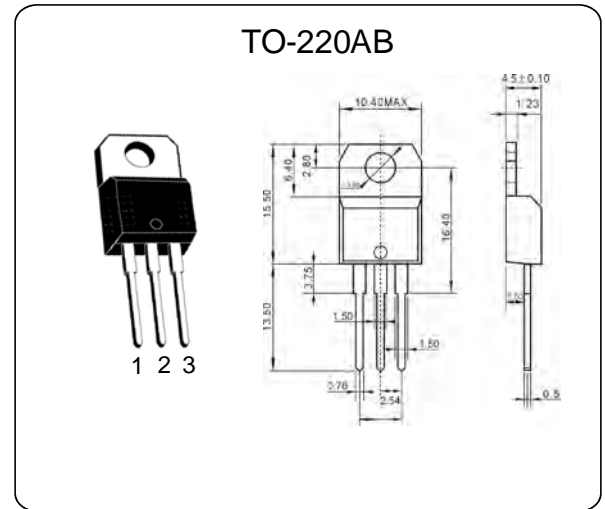


Bi-Directional Triode Thyristor

Designed for high performance full-wave ac control applications where high noise immunity and high commutating di/dt are required.

Features

- Blocking Voltage to 800 V
- On-State Current Rating of 6A RMS at 100°C
- Uniform Gate Trigger Currents in Three Quadrants
- High Immunity to dV/dt-1500V/us minimum at 125°C
- Minimizes Snubber Networks for Protection
- Industry Standard TO-220AB Package
- High Commutating di/dt- 4.0A/ms minimum at 125°C
- Internally Isolated (2500VRMS)
- These are Pb-Free Devices



Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
I _{T(RMS)}	RMS on-state current(full sine wave)	TO-220AB TC=110 °C	6	A
		TO-220AB Ins. TC=100 °C		
I _{TSM}	Non repetitive surge peak on-state current(full cycle, T _j initial=25 °C)	F=50Hz t=20ms	60	A
		F=60Hz t=16.7ms	65	
I ² t	I ² t Value for fusing	tp=10ms	31	A ² s
DI/DT	Critical rate of rise of on-state current I _G =2X _{IGT} , tr≤100ns	F=120Hz T _j =125 °C	50	A/us
I _{GM}	Peak gate current	tp=20us T _j =125 °C	2	A
P _{G(AV)}	Average gate power dissipation	T _j =125 °C	0.5	W
T _{stg}	Storage junction temperature range		-40 to +150	°C
T _j	Operating junction temperature range		-40 to +125	



BTA06-800B

Electrical Characteristics (T_j=25°C, unless otherwise specified)

Snubberless™ and Logic Level(3 quadrants)

Symbol	Test conditions	Quadrant	BTA06-800B		Unit
I _{GT} (1)	V _D =12V R _L =30Ω	I - II -III -IV	MAX	50	mA
V _{GT}		I - II -III -IV	MAX	1.3	V
V _{GD}	V _D =V _{DRM} R _L =3.3KΩT _j =125°C	I - II -III -IV	MIN	0.2	V
I _H (2)	IT=100mA		MAX	50	mA
I _L	I _G =1.2I _{GT}	I - II -III -IV	MAX	70	mA
		II		80	
Dv / Dt(2)	V _D =67%V _{DRM} Gate open T _j =125°C		MIN	1000	V/us
(DI/dt)c(2)	(Dv/dt)c=0.1 V/us T _j =125°C		MIN	-	A/ms
	(Dv/dt)c=10V/us T _j =125°C			-	
	Without snubber T _j =125°C			7	

Standard (4Quadrants)

Symbol	Test conditions	Quadrant	BTA06-800B		Unit
I _{GT} (1)	V _D =12V R _L =30Ω	I - II -III	MAX	50	mA
		IV		100	
V _{GT}		ALL	MAX	1.3	V
V _{GD}	V _D =V _{DRM} R _L =3.3KΩT _j =125°C	ALL	MIN	0.2	V
I _H (2)	IT=500mA		MAX	50	mA
I _L	I _G =1.2I _{GT}	I -III- IV	MAX	50	mA
		II		100	
(DI/dt)(2)	V _D =67%V _{DRM} Gate open T _j =125°C		MIN	400	V/us
(DI/dt)c(2)	(Dv/dt)c=3.5 A/ms T _j =125°C		MIN	10	V/us

Static Characteristics

Symbol	Test conditions			Value	Unit
V _{TM} (2)	ITM=5A tp=380us	T _J =25°C	MAX	1.70	V
V _{to} (2)	Threshold voltage	T _J =125°C	MAX	0.85	V
R _d (2)	Dynamic resistance	T _J =125°C	MAX	50	mΩ
I _{DRM}	V _{DRM} =V _{R_{RRM}}	T _J =25°C		5	uA
I _{R_{RRM}}		T _J =125°C	MAX	1	mA
V _{DRM} /V _{R_{RRM}}	Voltage	T _J =25°C	MIN	800	V

Note 1: minimum I_{GT} is guaranteed at 5% of I_{GT} max

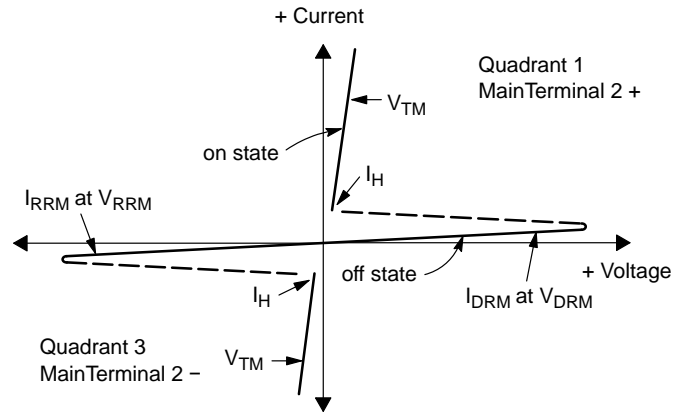
Note 2: for both polarities of A2 referenced to A1

Thermal Resistances

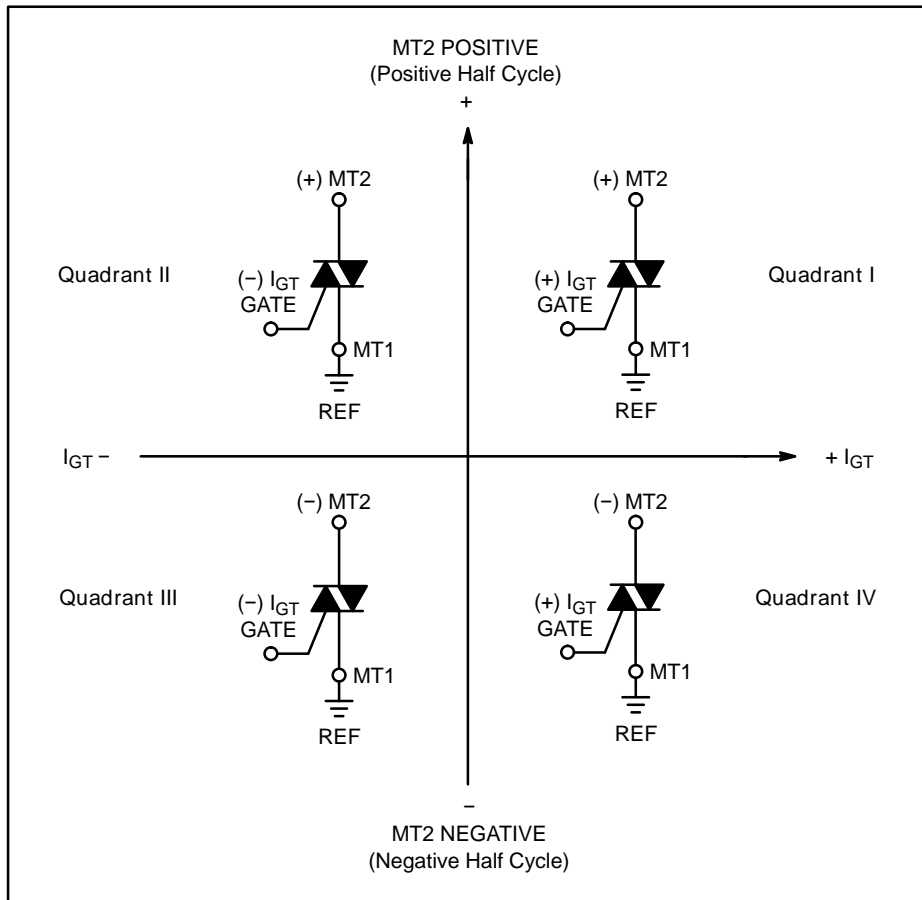
Symbol	Parameter	Value	Unit
R _{th} (J-C)	Junction to case(AC)	3.0	°C/W

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in-phase signals (using standard AC lines) quadrants I and III are used.

Description

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

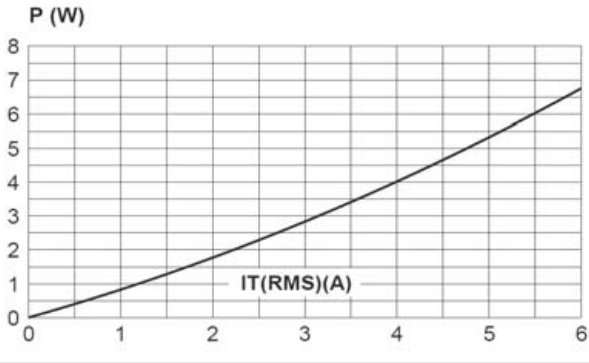


Fig. 2: RMS on-state current versus case temperature (full cycle).

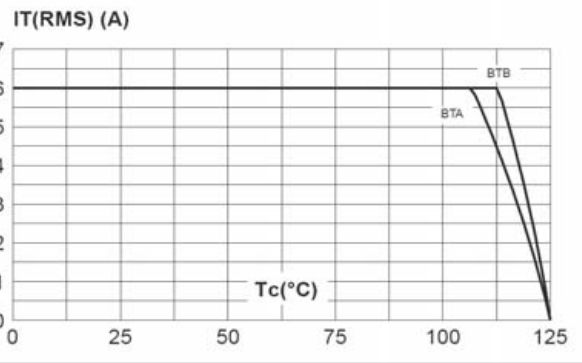


Fig. 3: Relative variation of thermal impedance versus pulse duration.

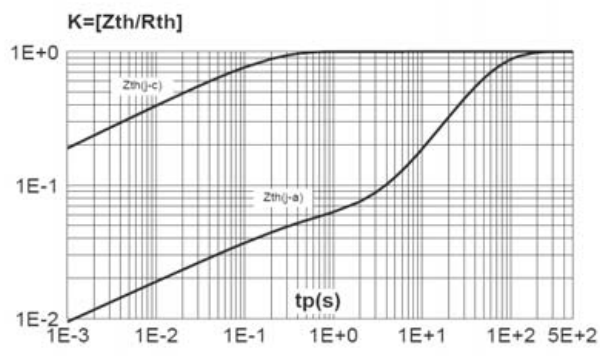


Fig. 4: On-state characteristics (maximum values).

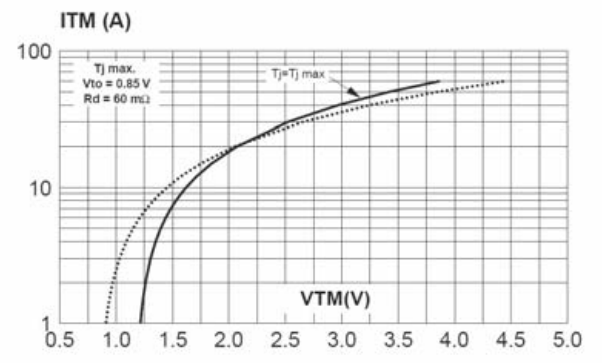


Fig. 5: Surge peak on-state current versus number of cycles.

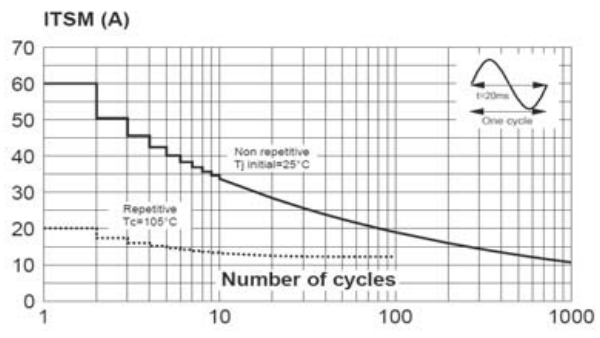
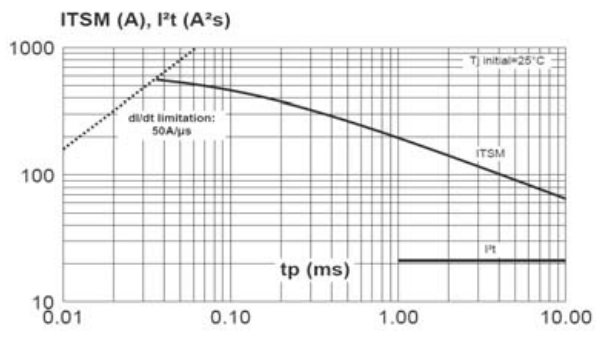


Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10\text{ms}$, and corresponding value of I^2t .



Description

Fig. 7: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).

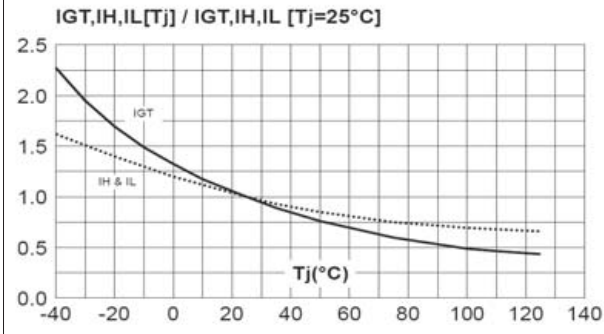


Fig. 8-1: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values). Snubberless & Logic Level Types

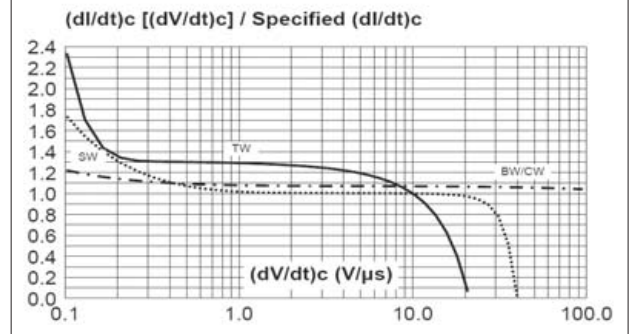


Fig. 8-2: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values). Standard Types

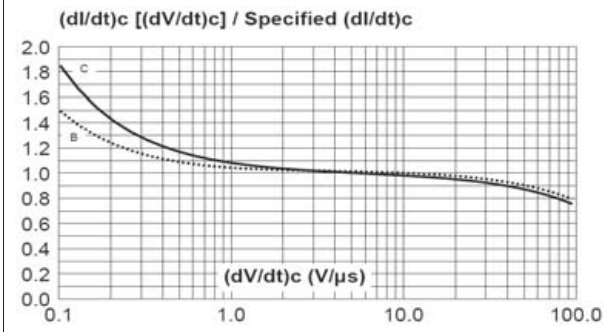


Fig. 9: Relative variation of critical rate of decrease of main current versus junction temperature.

