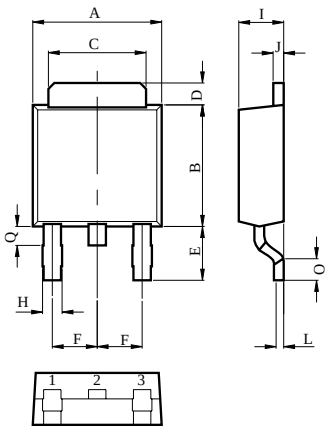
Bi-Directional Triode Thyristor

Designed for high performance full-wave ac control applications where high noise immunity and high commutating di/dt are required.



DIM	MILLIMETERS
A	6 50 ± 0 2
B	5 60 ± 0 2
C	5 20 ± 0 2
D	1 50 ± 0 2
E	2 70 ± 0 2
F	2 30 ± 0 1
H	1 00 MAX
I	2 30 ± 0 2
J	0 5 ± 0 1
L	0 50 ± 0 10
O	1 6 ± 0 2
Q	0 95 MAX

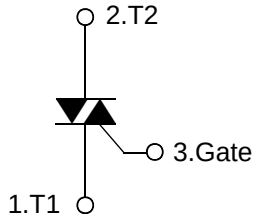
1 ANODE (T1)
2 ANODE (T2)
3 GATE

D-PAK (TO-252)

Features

- Blocking Voltage to 600 V
- On-State Current Rating of 8A RMS at 100℃
- Uniform Gate Trigger Currents in Three Quadrants
- High Immunity to dV/dt- 1500V/us minimum at 125℃
- Minimizes Snubber Networks for Protection
- Industry Standard TO-252 Package
- High Commutating dI/dt- 4.0A/ms minimum at 125℃
- These are Pb-Free Devices

Symbol



Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current(full since wave)	TO-252	TC=110℃	8	A
I_{TSM}	Non repetitive surge peak on-state current(full cycle, Tj initial=25℃)	F=50Hz	t=20ms	80	A
		F=60Hz	t=16.7ms	84	
I^2t	I^2t Value for fusing	tp=10ms		36	A^2s
DI/DT	Critical rate of rise of on-state current IG=2X$I_{GT,tr\leq100ns}$	F=120Hz	Tj=125℃	50	A/us
I_{GM}	Peak gate current	tp=20us	Tj=125℃	4	A
$P_{G(AV)}$	Average gate power dissipation		Tj=125℃	1	W
T_{stg}	Storage junction temperature range			-40 to +150	℃
T_j	Operating junction temperature range			-40 to +125	

Electrical Characteristics (Tj=25℃,unless otherwise specified)

Snubberless™ and Logic Level(3 quadrants)

Symbol	Test conditions	Quadrant	BT08D-600S		Unit
I_{GT}(1)	V_D=12V R_L=30Ω	Ⅰ-Ⅱ-Ⅲ-Ⅳ	MAX	5	mA
V_{GT}		Ⅰ-Ⅱ-Ⅲ-Ⅳ	MAX	1.3	V
V_{GD}	V_D=V_{DRM} R_L=3.3KΩTj=125℃	Ⅰ-Ⅱ-Ⅲ-Ⅳ	MIN	0.2	V
IH(2)	IT=100mA		MAX	50	mA
IL	I_G=1.2I_{GT}	Ⅰ-Ⅱ-Ⅲ-Ⅳ	MAX	70	mA
		Ⅱ		80	
Dv / Dt(2)	VD=67%V_{DRM} Gate open Tj=125℃		MIN	1000	V/us
(Dl/dt)c(2)	(Dv/dt)c=0.1 V/us Tj=125℃		MIN	-	A/ms
	(Dv/dt)c=10V/us Tj=125℃			-	
	Without snubber Tj=125℃			7	

Standard (4Quadrants)

Symbol	Test conditions	Quadrant	BT08D-600S		Unit
IGT(1)	VD=12V RL=30Ω	Ⅰ-Ⅱ-Ⅲ	MAX	5	mA
		Ⅳ		100	
VGT		ALL	MAX	1.3	V
VGD	VD=VDRM RL=3.3KΩTj=125℃	ALL	MIN	0.2	V
IH(2)	IT=500mA		MAX	50	mA
IL	IG=1.2IGT	Ⅰ-Ⅲ-Ⅳ	MAX	50	mA
		Ⅱ		100	
(Dl/dt)(2)	VD=67%VDRM Gate open Tj=125℃		MIN	400	V/us
(Dl/dt)c(2)	(Dv/dt)c=3.5 A/ms Tj=125℃		MIN	10	V/us

Static Characteristics

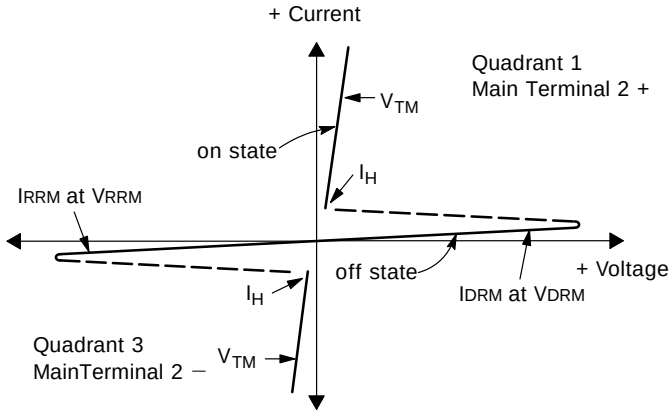
Symbol	Test conditions			Value	Unit
VTM(2)	ITM=11A tp=380us	TJ=25℃	MAX	1.55	V
Vto(2)	Threshold voltage	TJ=125℃	MAX	0.85	V
Rd(2)	Dynamic resistance	TJ=125℃	MAX	50	mΩ
I_{DRM}	V_{DRM}=V_{RRM}	TJ=25℃		5	uA
I_{RRM}		TJ=125℃	MAX	1	mA
V_{DRM}/V_{RRM}	Voltage	TJ=25℃	MIN	600	V

Note 1: minimum IGT is guaranted at 5% of IGT max

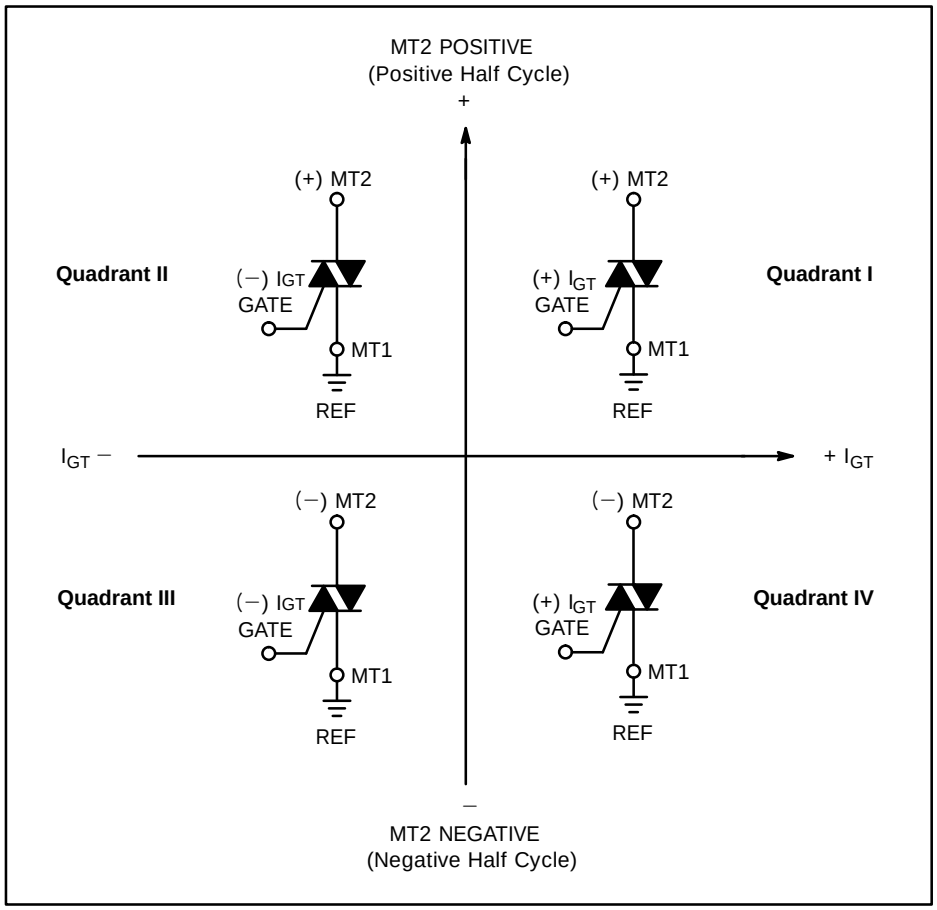
Note 2: for both polarities of A2 referenced to A1

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off StateVoltage
I_{RRM}	Peak ReverseBlockingCurrent
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in−phase signals (using standard AC lines) quadrants I and III are used.

Description

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

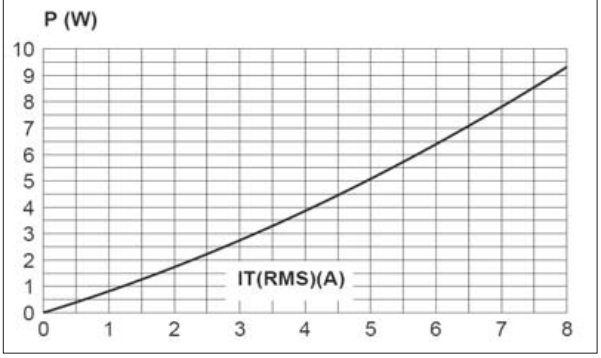


Fig. 2-1: RMS on-state current versus case temperature (full cycle).

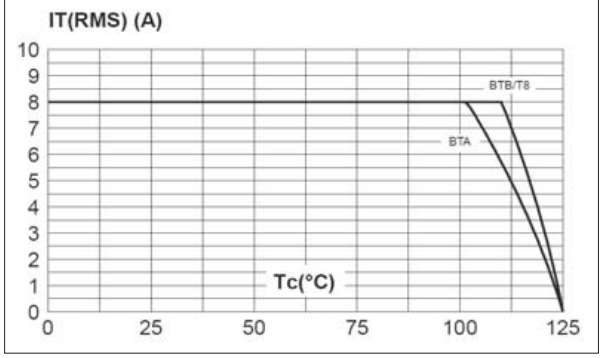


Fig. 2-2: RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35µm),full cycle.

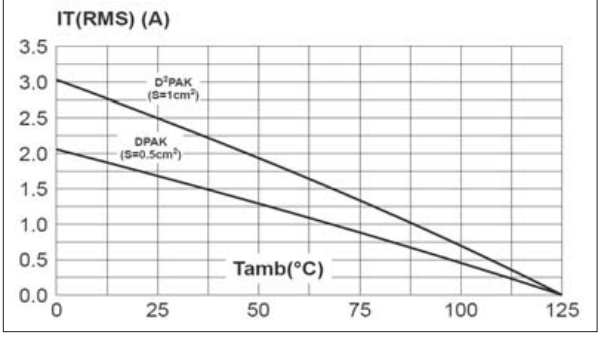


Fig. 3: Relative variation of thermal impedance versus pulse duration.

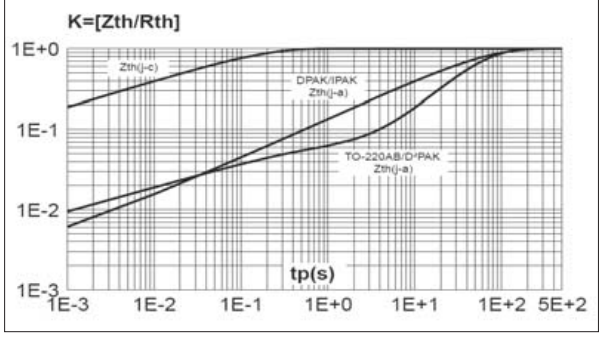


Fig. 4: On-state characteristics (maximum values).

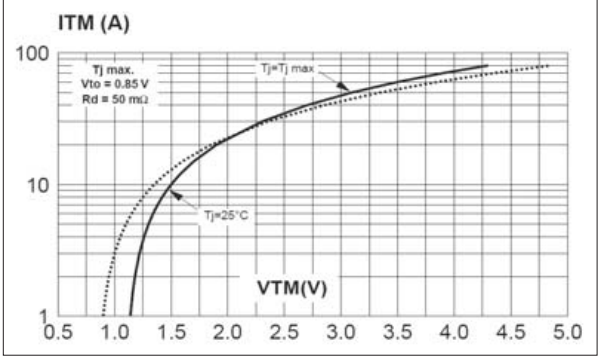
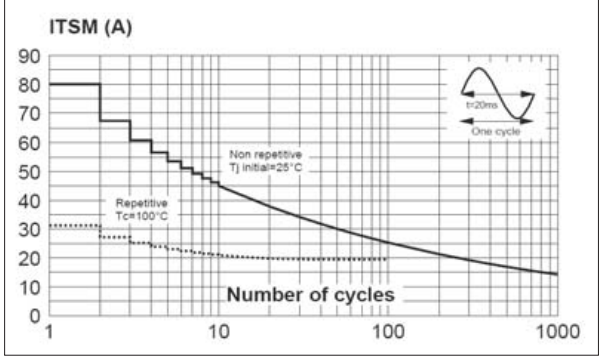


Fig. 5: Surge peak on-state current versus number of cycles.



Description

Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10ms, and corresponding value of I²t.

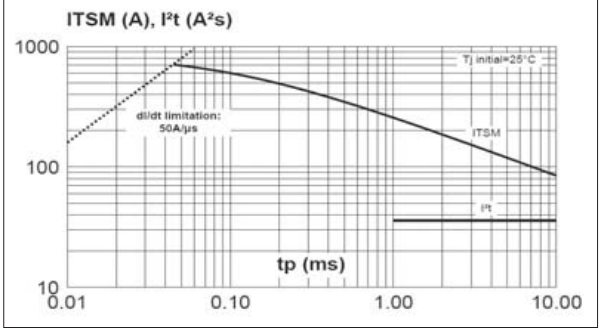


Fig. 7: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).

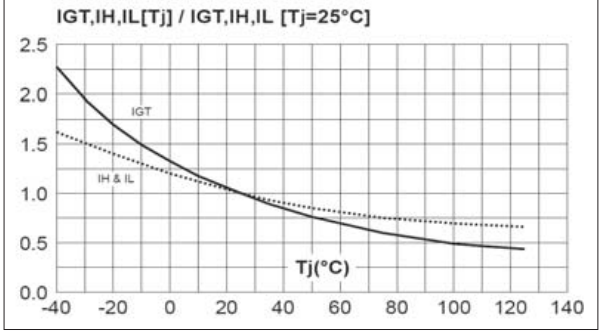


Fig. 8-1: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values). Snubberless & Logic Level Types

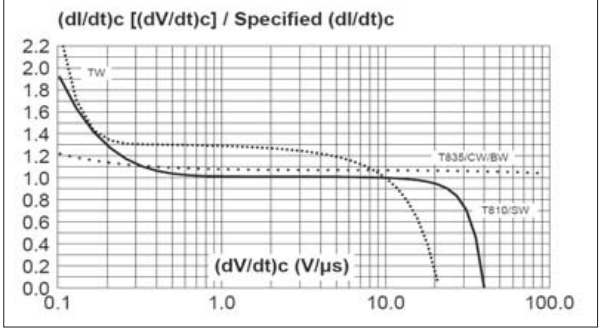


Fig. 8-2: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values). Standard Types

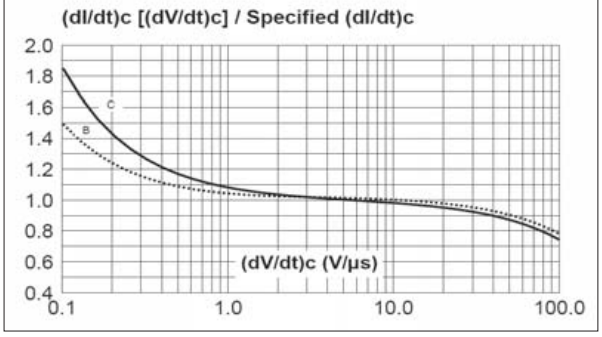


Fig. 9: Relative variation of critical rate of decrease of main current versus junction temperature.

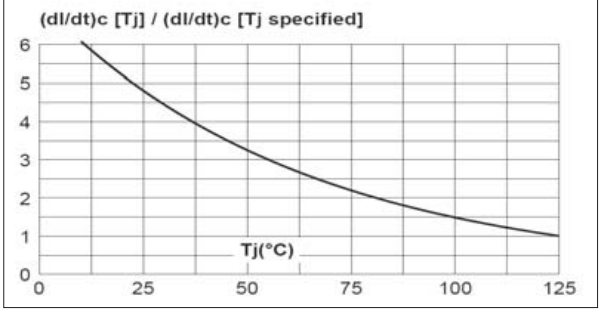


Fig. 10: DPAK and D²PAK Thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35 µm).