PWM Current-Mode Controller for Free-Running Quasi-Resonant Operation

General Description

FC8206ASG combines a true current mode modulator and a demagnetization detector which ensures full borderline/critical Conduction Mode in any load/line conditions together with minimum drain voltage switching (Quasi Resonant operation).

For FC8206ASG, an internal 7.5u s timer prevents the free run frequency to exceed 120 kHz (therefore below the 150 kHz CISPR-22 EMI starting limit).

FC8206ASG optimized for high performance, low standby power (<100mW) and cost effective offline flyback. converter applications in 40W ~ 100W range.

Features

- Free-Running Borderline/Critical Mode Quasi-Resonant Operation
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- 4.0 ms Soft Start Reducing MOSFET VDS Stress
- Built-in leading edge blanking (LEB)
- Internal Synchronized Slope Compensation
- Good protection coverage with auto self-recovery

＊ VCC Under Voltage Lockout with Hysteresis (UVLO)

＊ Over Temperature Protection (OTP) auto-recovery

＊ Cycle-by-cycle over current threshold setting for constant output power limiting over universal input voltage range

＊ Overload Protection (OLP) with auto-recovery

＊ VCC Over voltage Protection(OVP) with auto-recovery

＊ CS floating protection with auto-recovery

＊ CS short protection with auto-recovery

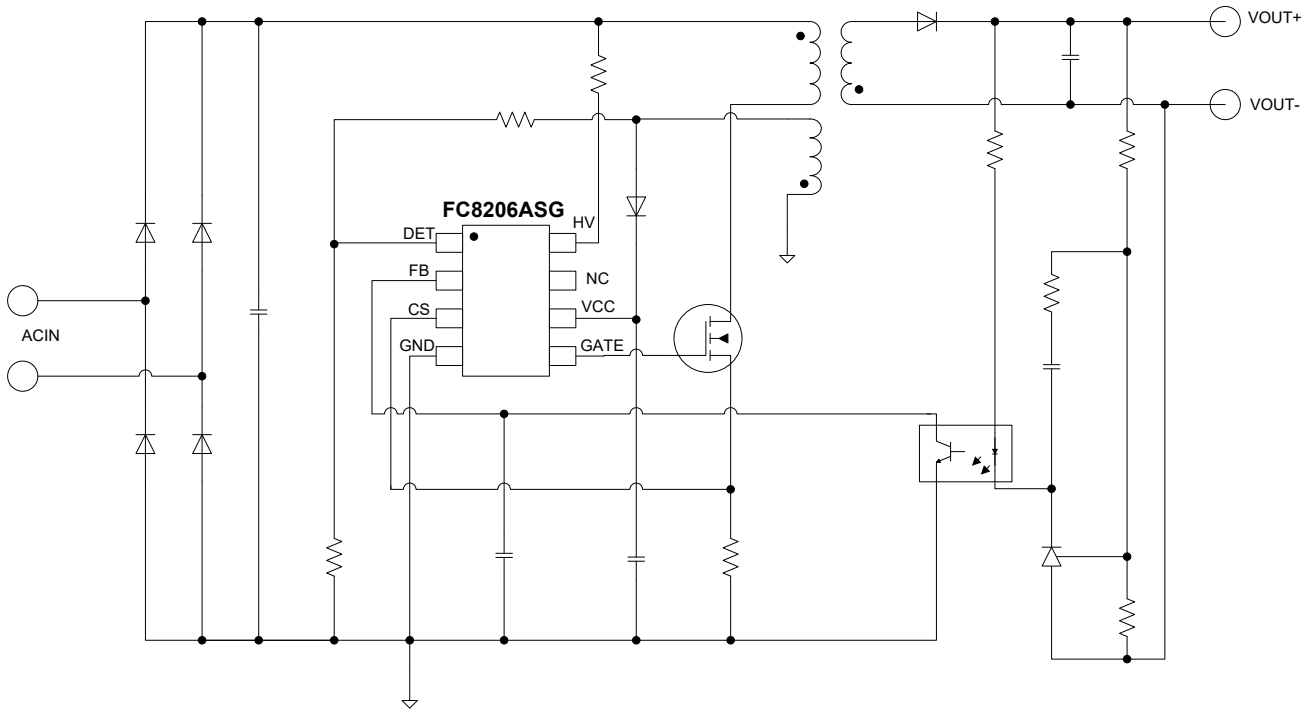
Typical Application

- AC-DC Adapters for Notebooks, etc.
- Offline Battery Chargers
- Consumer Electronics (DVD Players, Set Top Boxes, TVs, etc.)
- Auxiliary Power Supplies (USB, Appliances, TVs, etc.)

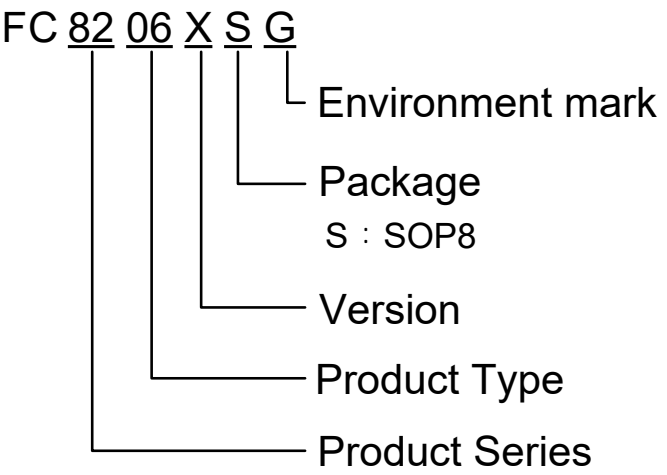
Package

- 8-pin SOP8

Typical Application Circuit

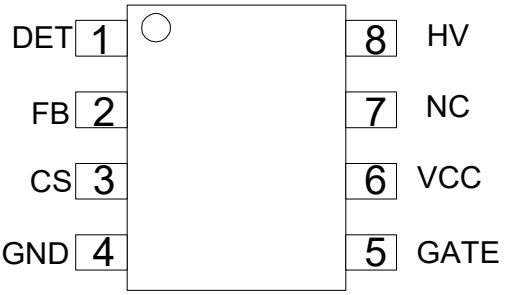


Selection Guide



product series	product description
FC8206ASG	Package：SOP8

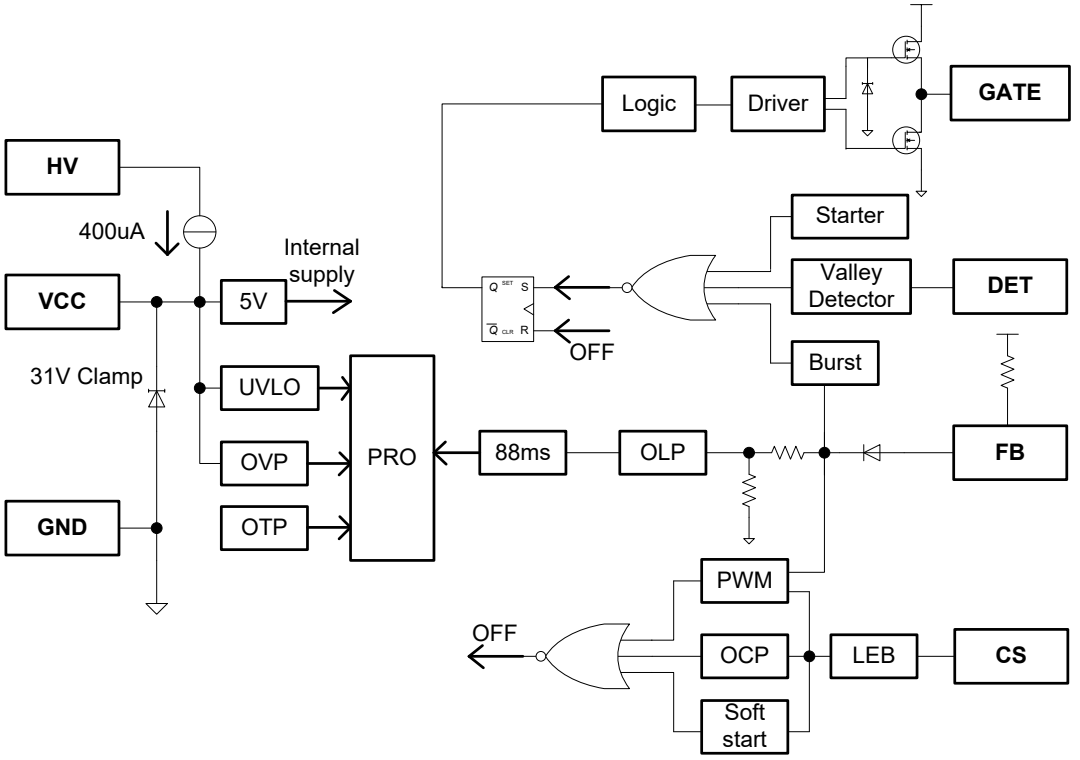
Pin Configuration



Pin Assignment

Pin Num.	Symbol	Function
1	DET	Valley detector pin.Connected to the auxiliary winding of the transformer.
2	FB	Voltage feedback pin, by connecting a photo-coupler to control the duty cycle.
3	CS	Current sense input pin. Connected to MOSFET current sensing resistor node.
4	GND	Ground
5	GATE	The driver's output to an external MOSFET.
6	VCC	Chip DC power supply pin.
7	NC	NC
8	HV	Connected to the high voltage rail, this pin injects a constant current into the VCC bulk capacitor and ensures a clean lossless startup sequence.

Block Diagram



Absolute Maximum Ratings

Parameter	Range	Unit
VCC DC Supply Voltage	30	V
DRAIN DC Supply Voltage	-0.3 ~ 650	V
VCC Clamp Current	10	mA
V_{FB} /V_{CS}/V_{DET} (FB/CS/DET Input Voltage)	-0.3 ~ 7	V
$R_{\theta JA}$ thermal Resistance(Junction to air)	150	°C/W
P_D Continuous Total Power Dissipation	0.9	W
Min/Max Operating Junction Temperature T_J	-40 ~ 150	°C
Min/Max Storage Temperature Tstg	-55 ~ 150	°C
Soldering temperature and time	+260（Recommended 10S）	°C

Caution: The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

Recommended working condition

Parameter	Range	Units
Power supply voltage, VCC	10 ~ 30	V
Operating temperature	-20 ~ 85	℃

Electrical Characteristics

(For typical values T_A =25 °C, for min/max values T_A = 0°C to +125°C, Max T_A = 150°C, VCC= 16V unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Internal Startup Current Source(HV)						
I_{Start}	High Voltage Current Source	V_{HV} = 30 V	-	400	-	μA
Supply Voltage (VCC)						
$I_{Startup}$	VCC Start up Current	VCC= $UVLO_{OFF}$ -1V, Measure leakage current into VCC	-	5	20	μA
$I_{VCC\_Operation}$	Operation Current	V_{FB}=3V	-	1.5	3.5	mA
$UVLO_{ON}$	VCC Under Voltage Lockout Enter		7.5	8.5	9.5	V
$UVLO_{OFF}$	VCC Under Voltage Lockout Exit (Recovery)		13.5	14.5	15.5	V
$VCC_{\_Clamp}$		I_{VCC} = 10 mA	31	34	36	V
OVP_{ON}	VCC Over voltage protection enter	CS=0V,FB=3V Ramp up VCC until gate clock is off	30	33	35	V
OTP	Over temperature protection		-	145	-	℃
Feedback Input Section(FB Pin)						
V_{FB_Open}	V_{FB} Open Loop Voltage		4.5	5	5.5	V

I_{FB_Short}	FB pin short circuit current	Short FB pin to GND, measure current	0.4	0.5	0.6	mA
V_{REF_GREEN}	The threshold enter green mode		-	1.7	-	V
$V_{REF\_BURST\_H}$	The threshold exit burst mode		-	1.15	-	V
$V_{REF\_BURST\_L}$	The threshold enter burst mode		-	1.05	-	V
V_{TH_PL}	Power Limiting FB Threshold Voltage		-	3.7	-	V
T_{D_PL}	Power limiting Debounce Time		80	88	96	mS
Current Sense Input(CS Pin)						
T_ soft start			-	4	-	mS
T_blanking	Leading edge blanking time		-	300	-	nS
T_{D_OC}	Over Current Detection and Control Delay	From over current occurs till the gate drive output start to turn off	-	120	-	nS
V_{TH_OC}	Internal current limiting threshold voltage	FB=3.3V	0.8	0.85	0.9	V
Valley detector(DET)						
T_{D_DET}	Valley detector delay		-	300	-	nS
Toff_min	Minimum Toff		7	7.5	8.5	uS
Gate driver(GATE)						
$T_{\_R}$	Output rising time	1V-12V@CL=3nF	150	-	-	nS
$T_{\_F}$	Output falling time	1V-12V@CL=3nF	100	-	-	nS
$V_{\_CLAMP}$	Output clamp voltage		-	16	20	V

Operation Description

FC8206ASG is a highly integrated PWM current mode controller for free running quasi resonant operation for high performance, low standby power (<100mW) and cost effective offline flyback converter applications in 40W ~ 60W range.

Startup Sequence

When the power supply is first powered from the mains outlet, the internal current source (typically 0.4mA) is biased and charges up the VCC capacitor. When the voltage on this VCC capacitor reaches the VCCON level (typically 14.5V), the current source turns off and no longer wastes any power. At this time, the VCC capacitor only supplies the controller and the auxiliary supply is supposed to take over before VCC collapses below VCCOFF .

Quasi Resonant Operation

The core reset detection is done by monitoring the voltage activity on the auxiliary winding. This voltage features a FLYBACK polarity. The typical detection level is fixed at 50 mV. An internal timer prevents any restart within 7.5 us further to the driver going low transition for FC8206ASG.This prevents the switching frequency to exceed (1.0/TON + Tbank) but also avoid false leakage inductance tripping at turn off. In some cases, the leakage inductance kick is so energetic, that a slight filtering is necessary.

By delaying the turn on event, it is possible to restart the MOSFET in the minimum of the drain source wave, ensuring reduced EMI/video noise perturbations and high efficiency.

Extended Burst Mode Operation

At zero load or light load condition, majority of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below burst mode threshold level and device enters Burst Mode control. The Gate drive output switches only when VCC voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend. The nature of high frequency switching also reduces the audio noise at any loading conditions.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in FC8206ASG. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to Snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limiting comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Gate Drive

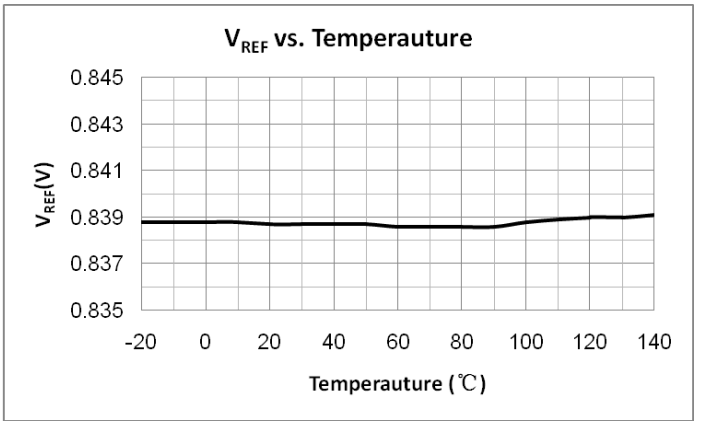
The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI. A good trade-off is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

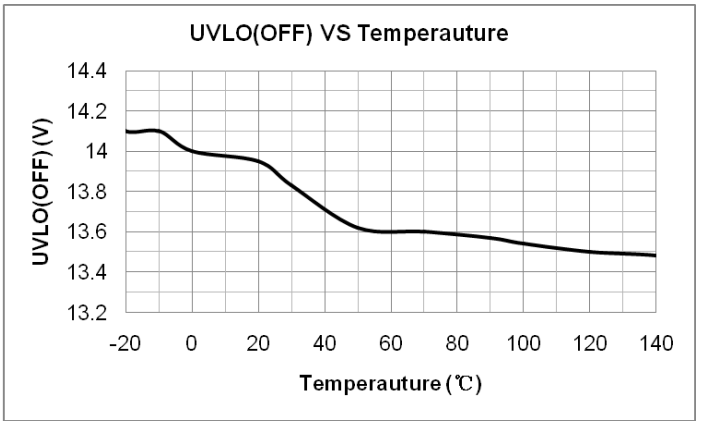
Protection Controls

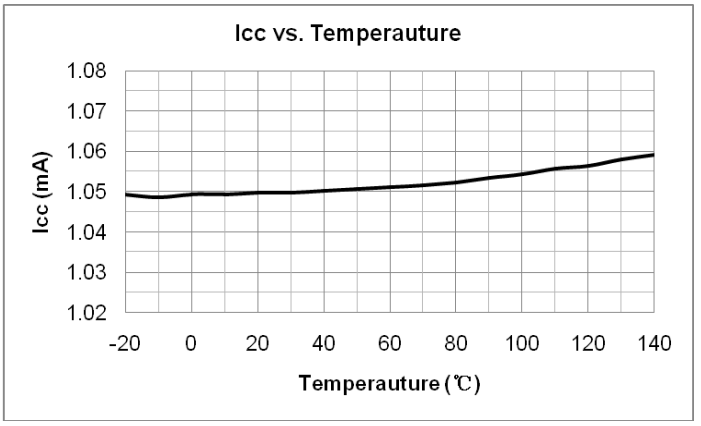
Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), CS short protection, CS floating protection, over temperature protection (OTP), fixed or adjustable over voltage protection (OVP), and Under Voltage Lockout on VCC (UVLO).

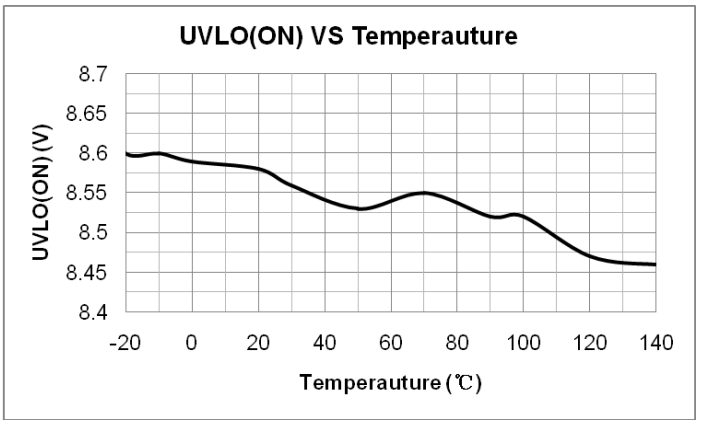
Typical performance characteristics

VCC= 16V, T_A = 25℃ condition applies if not otherwise noted



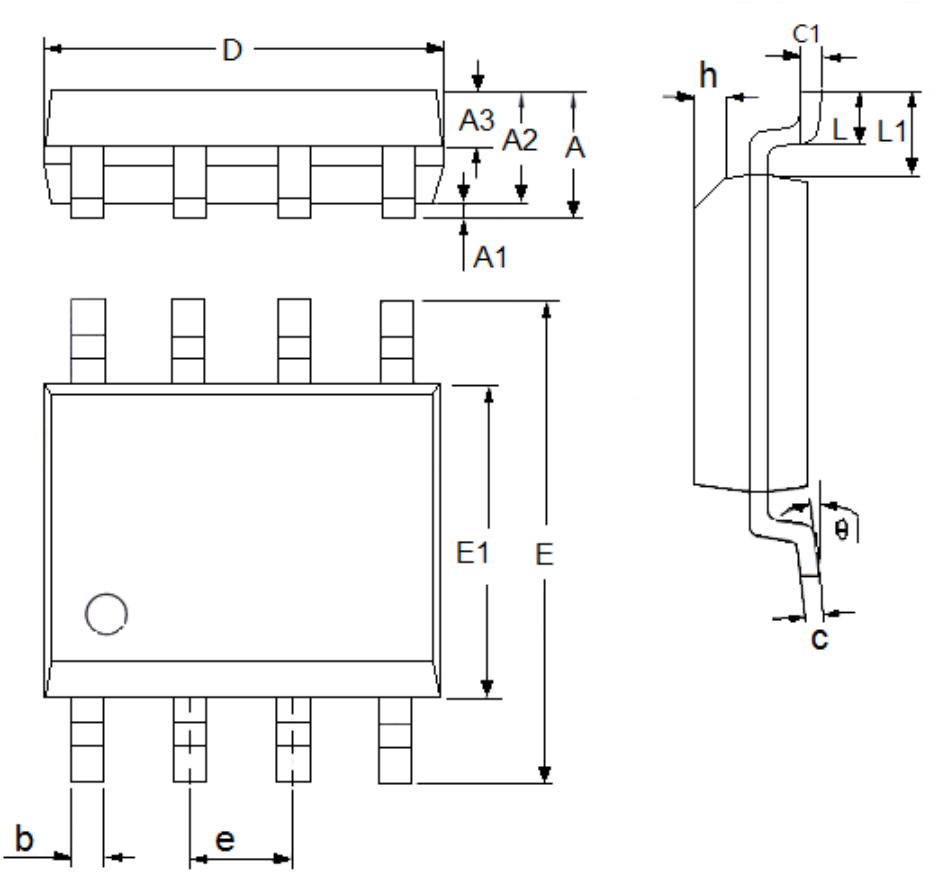






Packaging Information

● **SOP8**



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	1.3	1.8	0.0512	0.0709
A1	0.05	0.25	0.002	0.0098
A2	1.25	1.65	0.0492	0.065
A3	0.5	0.7	0.0197	0.0276
b	0.3	0.51	0.0118	0.0201
c	0.17	0.25	0.0067	0.0098
D	4.7	5.1	0.185	0.2008
E	5.8	6.2	0.2283	0.2441
E1	3.8	4	0.1496	0.1575
e	1.27(TYP)		0.05(TYP)	
h	0.25	0.5	0.0098	0.0197
L	0.4	1.27	0.0157	0.05
L1	1.04(TYP)		0.0409(TYP)	
θ	0	8°	0	8°
c1	0.25(TYP)		0.0098(TYP)	