High Efficiency QR Boost PFC Constant Voltage Power Switch

FEATURES

- **Quasi-Resonant for High Efficiency**
- **Support Single Windings Design**
- **Built-in HV MOSFET and Power Supply Circuit**
- **Low Cost Boost APFC Solution**
- **PF>0.9 and THD<10% with Universal Input**
- **Fast Startup < 200ms**
- **High Precision CV Regulation**
- **Very Low VDD Operation Current**
- **Excellent Line and Load Regulation**
- **Built-in Protections:**
  - **Output Over Voltage Protection (OVP)**
  - **Output Under Voltage Protection(UVP)**
  - **Cycle-by-Cycle Current Limiting (OCP)**
  - **Leading Edge Blanking (LEB)**
  - **On-Chip Thermal Fold Back (OTP)**
- **Available in SOP-7 and DIP-8 Package**

GENERAL DESCRIPTION

FC1511X is a highly integrated Boost PFC Constant Voltage Power Switch. The IC utilizes Quasi-Resonant (QR) Boost topology with active PFC control for high PF, low THD, and high efficiency.

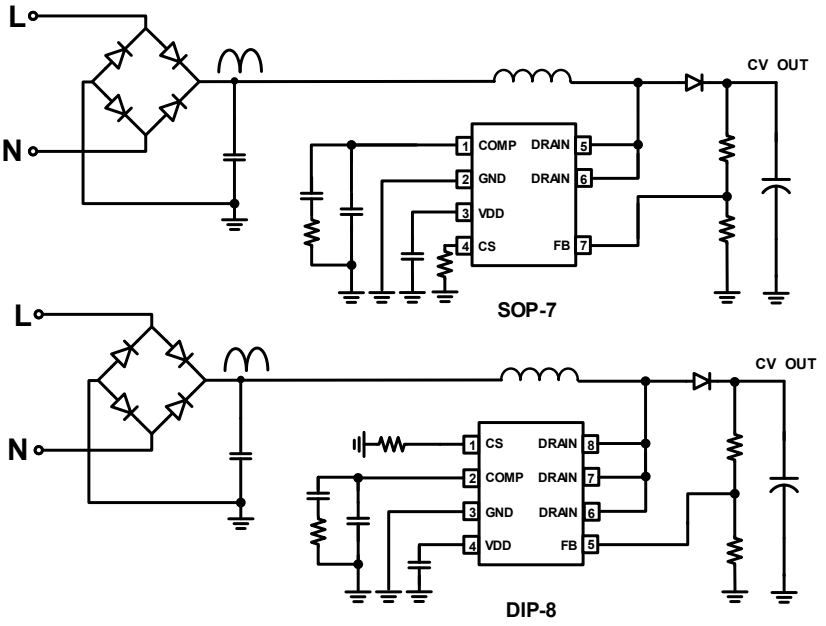
FC1511X integrates with demagnetization signal detection technology, high voltage MOSFET, high voltage startup and IC power supply circuit, which eliminates auxiliary windings for demagnetization detection and power supply, simplifies system design and lower cost.

FC1511X integrates functions and protections of Under Voltage Lockout (UVLO), Cycle-by-cycle Current Limiting (OCP), Thermal Foldback (OTP), Output Over Voltage Protection (OVP), Output Under Voltage Protection (UVP) etc.

APPLICATIONS

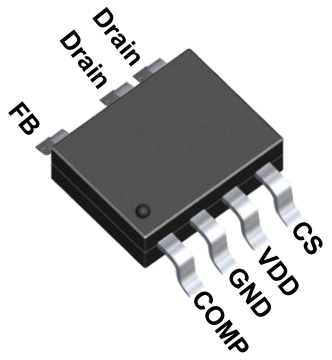
- **Constant Voltage PFC Application**

TYPICAL APPLICATION CIRCUIT

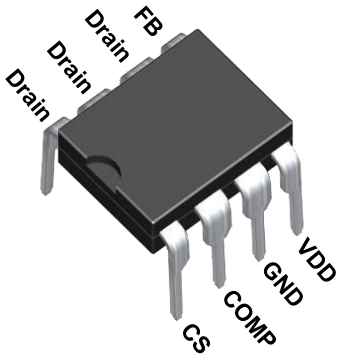


High Efficiency QR Boost PFC Constant Voltage Power Switch

Pin Configuration

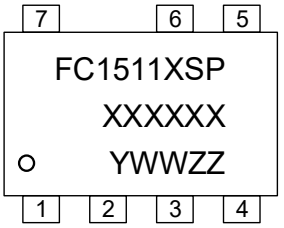


SOP-7



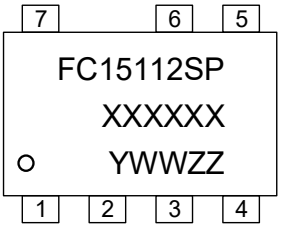
DIP-8

Marking Information



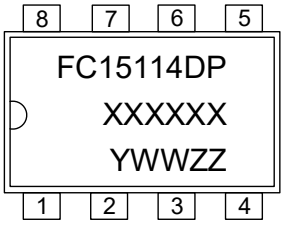
XXXXXX : Wafer for Code
Y : Year Code
WW : Week Code，01-52
ZZ : Serial Number，01-99 or A0-ZZ
X : 1 - FC15111
3 - FC15113
4 - FC15114

SOP-7



XXXXXX : Wafer for Code
Y : Year Code
WW : Week Code，01-52
ZZ : Serial Number，01-99 or A0-ZZ
F, S: Control Number, 1-9 or A-Z, a-z

SOP-7



XXXXXX : Wafer for Code
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DIP-8

Pin Description

Pin Number (SOP-7)	Pin Number (DIP-8)	Pin Name	I/O(1)	Description
1	2	COMP	I	Loop Compensation Pin.
2	3	GND	P	IC Ground Pin
3	4	VDD	P	IC Power Supply Pin. Connect a >2.2μF Capacitor between this Pin and GND
4	1	CS	P	Current Sense Input Pin
5, 6	6, 7, 8	Drain	P	Internal Power MOSFET Drain Pin
7	5	FB	I	Output Voltage Setting Pin, Steady State Setting at 2.4V

(1) I - Input; P - Power

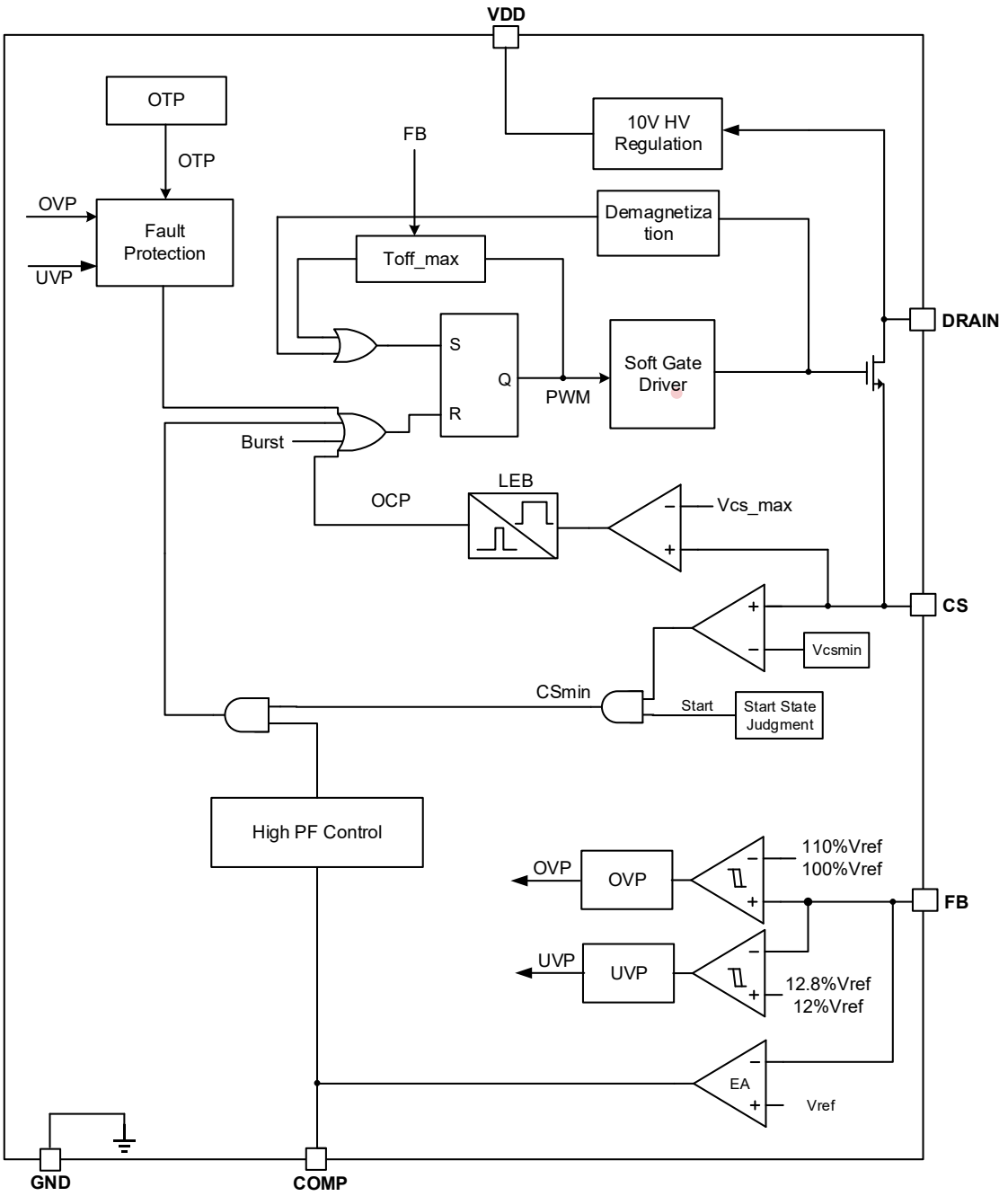
High Efficiency QR Boost PFC Constant Voltage Power Switch

Ordering Information

Part Number(2)	Description
FC15111SPA/FC15112SPA/FC15113SPA/FC15114SPA	SOP-7, Pb Free in T&R, 4000 Pcs/Reel
FC15114DP	DIP-8, Pb Free, 50 Pcs/Tube

(2) Suffix "A" – Tape & Reel.

Block Diagram



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Absolute Maximum Ratings(3)

Parameter	Value	Unit
DRAIN Pin Voltage Range	-0.3 to 500	V
VDD DC Supply Voltage	self-limited	V
VDD DC Clamp Current	10	mA
CS, FB, COMP Voltage Range	-0.3 to 7	V
P_{Dmax}, Power Dissipation @T_A=50℃ (SOP-7) (4)	0.6	W
θ_{JA}, Thermal Resistance---Junction to Ambient (SOP-7) (4)	165	℃/W
P_{Dmax}, Power Dissipation @T_A=50℃ (DIP-8) (4)	0.9	W
θ_{JA}, Thermal Resistance---Junction to Ambient (DIP-8) (4)	105	℃/W
Maximum Junction Temperature	150	℃
Storage Temperature Range	-65 to 150	℃
Lead Temperature (Soldering, 10sec.)	260	℃
ESD Capability, HBM (Human Body Model)	3	kV

(3) Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

(4) Maximum Power dissipation P_{Dmax}= (T_{Jmax}-T_A)/θ_{JA}. As ambient temperature rises, P_{Dmax} will decrease.

Recommended Operation Conditions

Parameter	Value	Unit
Operating Junction Temperature	-40 to 125	℃

Electrical Characteristics (Ta = 25℃, VDD=10V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Section (VDD Pin)						
I_{VDD_st}	VDD Pin Start-up Current	VDD<V_{DD_Op}		300	700	μA
I_{VDD_Op}	Operation Current	Fsw=7kHz	80	200	350	μA
V_{DD_Op}	VDD Operation Voltage		9	10	11.5	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter		6.5	7.5	8	V
V_{DD_Clamp}	VDD Clamp Voltage	I(V_{DD}) = 5mA	13.5	14.1	15.5	V
Driver Section						
T_{dem_blank}	Turn Off Blanking Time(5)			2.5		μs
T_{on_max}	Maximum ON Time		20	30	40	μs

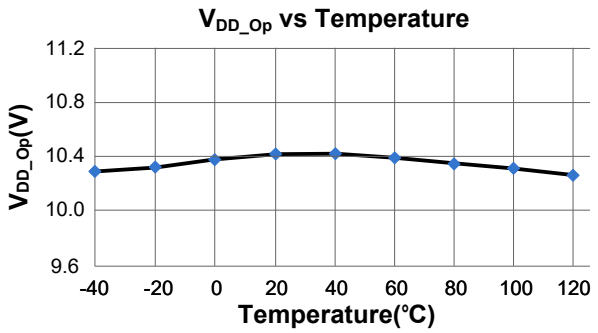
High Efficiency QR Boost PFC Constant Voltage Power Switch

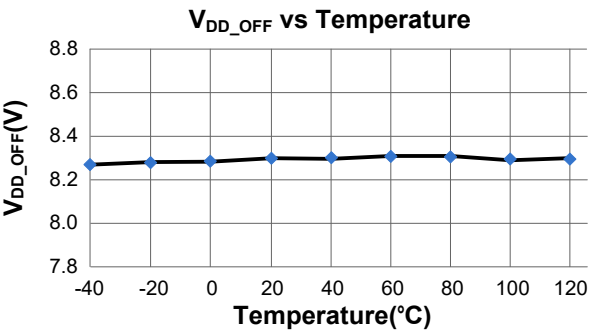
$T_{off\_max\_st}$	Maximum OFF Time at Startup		105	150	195	μs
T_{off_max}	Maximum OFF Time at Steady State		195	270	350	μs
F_{max}	Max. Switching Frequency			200		kHz
Current Sense Input Section (CS Pin)						
V_{cs_max}	Current Limiting Threshold		1.8	2	2.2	V
T_{D_OC}	Over Current Detection and Control Delay			100		ns
$V_{cs\_min\_st}$	Minimum Current Sensing Limit at Startup		0.6	0.67	0.73	V
V_{cs_min}	Minimum Current Sensing Limit at Steady State		90	100	110	mV
Output Protection Section (FB PIN)						
V_{ref}	Reference Voltage		2.35	2.4	2.45	V
$V_{FB\_OVP\_EN}$	Enter OVP Voltage	110% Ref	2.63	2.68	2.73	V
$V_{FB\_OVP\_EX}$	Exit OVP Voltage	100% Ref	2.35	2.4	2.45	V
$V_{FB\_OVP\_Deb}$	Debounce Time			10		μs
$V_{FB\_UVP\_EN}$	Enter UVP Voltage	12% Ref	0.25	0.3	0.35	V
$V_{FB\_UVP\_EX}$	Exit UVP Voltage	12.8% Ref		0.32		V
$V_{FB\_UVP\_Deb}$	Debounce Time			10		μs
CC Loop Compensation Section (COMP Pin)						
V_{comp_H}	COMP High Clamp Voltage			4.5		V
V_{comp_L}	COMP Low Clamp Voltage			1.2		V
Over Temperature Protection						
T_{OTP_EN}	Thermal Foldback Trigger Point(5)			150		℃
T_{OTP_EX}	OTP Recovery Threshold			140		℃
HV Startup and IC Supply Section (Drain Pin)						
I_{HV}	HV Charging Current	Drain = 20V		10		mA
I_{HV_leak}	Leakage Current of HV Charging Circuit		10	40	60	μA
Power MOSFET Section (Drain Pin)						
V_{BR}	Power MOSFET Drain Source Breakdown Voltage		500			V
R_{dson}	Static Drain-Source On Resistance	FC15111		9	11	Ω
		FC15112		5.8	6.5	Ω
		FC15113		2.8	3.5	Ω
		FC15114		1.9	2.3	Ω

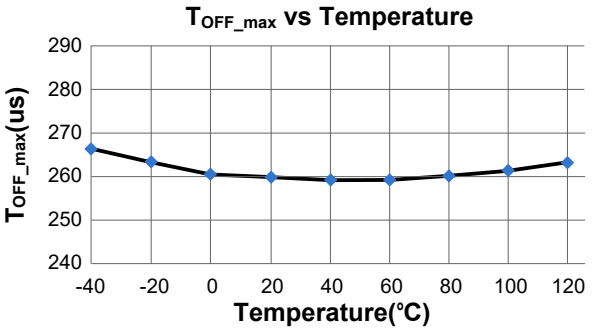
(5) Guaranteed by the Design.

High Efficiency QR Boost PFC Constant Voltage Power Switch

Typical Characteristic







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Operation Description

FC1511X is a highly integrated Boost PFC Constant Voltage Power Switch. The IC utilizes Quasi-Resonant (QR) Boost topology with active PFC control for high PF, low THD, and high efficiency.

- **10V Regulator**

In FC1511X, the 10V regulator charges VDD hold-up capacitor to 10V by drawing a current from the voltage on the DRAIN pin. Extremely low IC power consumption allows FC1511X to operate continuously from the current drawn from the DRAIN pin. A capacitor value about 2.2μF at least is sufficient for both high frequency decoupling and energy storage.

- **System Start-Up Operation**

After system power up, VDD hold up capacitor is charged by the internal HV startup circuit through DRAIN pin. When VDD pin voltage reaches the turn on threshold, the IC begins working. The COMP pin is pulled up to 1.2V quickly, then the IC begins to work at low switching frequency, the COMP pin voltage rises up gradually, thus the inductor peak current also rises up. The output voltage achieves a soft start without over shoot.

- **Constant Voltage (CV) Control**

The FC1511X samples the output voltage through the FB pin and compares it with the internal high-precision 2.4V reference to maintain a constant output voltage. The output voltage under closed loop control is determined by the following formula:

$$V_O(V)=\frac{V_{ref}}{R_{FB1}} X (R_{FB1}+R_{FB2})$$

In the equation above,

R_{FB1} --- the Resistor between FB pin and GND

R_{FB2} --- the Upper Voltage Divider Resistor

- **Leading Edge Blanking (LEB)**

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by the MOSFET parasitic capacitance and freewheeling diode reverse recovery current. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (300ns, typical), the PWM comparator is disabled and cannot switch off the gate driver.

- **Cycle-by-cycle Current Limit Protection (OCP)**

The FC1511X limits the maximum inductor current through the MOFET each time the power MOSFET is turned on. When the CS voltage exceeds the peak current reference Vcs_max, the power MOSFET is immediately turned off.

- **Demagnetization Detection**

FC1511X integrates demagnetization module which eliminates auxiliary windings to detect demagnetization signals for quasi-resonance control and lower cost.

- **Time Control**

In FC1511X, a blank time (typically 1μs) is implemented to suppress ringing when the power MOSFET is off to avoid OVP false triggering. The maximum OFF time in FC1511X is typically 270μs. FC1511X also integrates duty cycle clamping function. The maximum operation frequency is limited to less than 200 kHz.

- **Output Over Voltage Protection (OVP)**

The output voltage can be detected by the FB pin. When the FB voltage is higher than FB High Voltage Threshold voltage (VFB_H), the power MOSFET stops switching immediately. The output

over voltage is determined by：

$$V_{OVP}(V)=\frac{V_{FB\_H}}{R_{FB1}}X(R_{FB1}+R_{FB2})$$

where：

R_{FB1} --- the Resistor between FB pin and GND

R_{FB2} --- the Upper Voltage Divider Resistor

- **Light Load Mode**

When the FC1511X detects a light load, the system enters Burst mode to improve efficiency of light load and reduce system standby loss.

- **On Chip Thermal Foldback (OTP)**

FC1511X integrates thermal foldback function. When the IC temperature is over 150℃, the IC stops switching. When the IC temperature is under 140℃, the system restart. In this way, the system temperature is limited and system reliability is also improved.

- **Soft Totem-Pole Gate Driver**

FC1511X has a soft totem-pole gate driver with optimized EMI performance.

- **PCB Layout Guide**

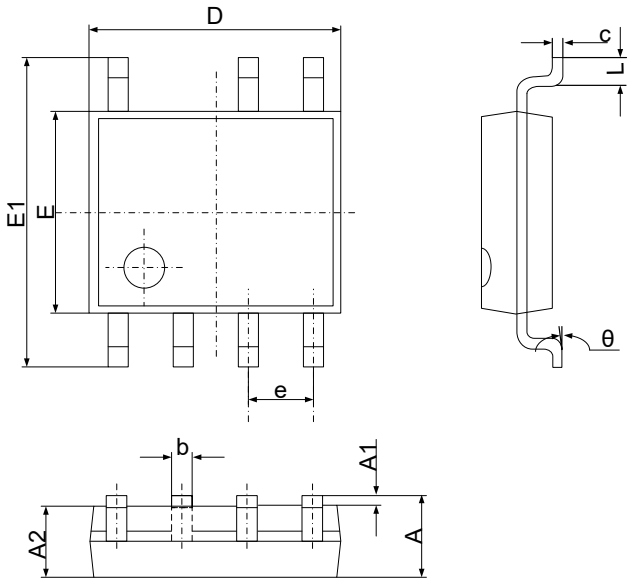
PCB layout is very important for reliable operation. Please follow guideline to optimize performance.

1. The area of main power switching loop should be as small as possible to reduce the EMI radiation, such as the inductor charging loop consisted by the EMI filter capacitor, inductor and ic; the inductor discharging loop consisted by the inductor, freewheeling diode and output capacitor.
2. Place the VDD Cap, COMP Cap, FB Res as close as the IC as possible.
3. The power ground of the current sampling resistor is as thick as possible and should be as close as the IC GND as possible.
4. Increase the copper area of the Drain pin to improve thermal performance.

High Efficiency QR Boost PFC Constant Voltage Power Switch

Package Dimension

SOP-7

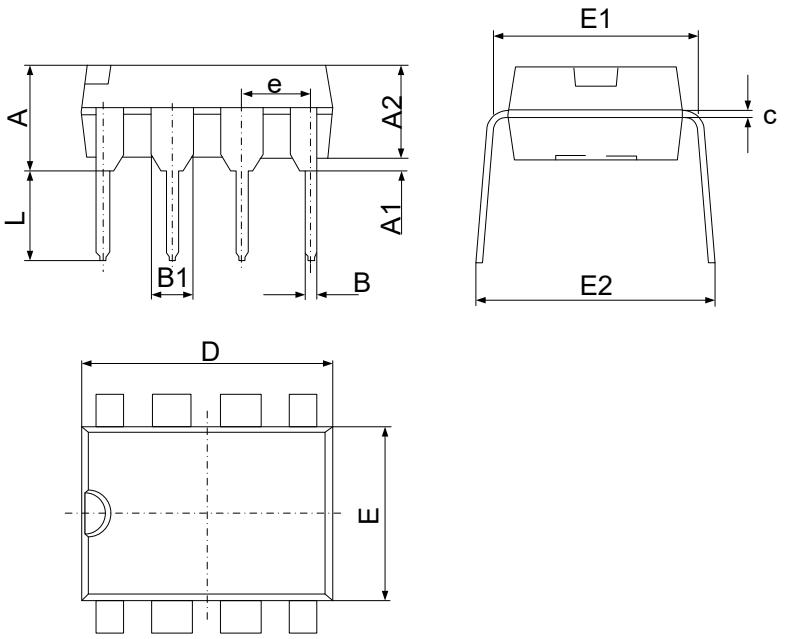


Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

High Efficiency QR Boost PFC Constant Voltage Power Switch

Package Dimension

DIP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	3.600	4.150	0.142	0.163
A1	0.510	-	0.020	-
A2	3.150	3.400	0.124	0.134
B	0.380	0.560	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
c	0.200	0.350	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.500	0.244	0.256
E1	7.620 (REF)		0.300 (REF)	
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	7.620	9.300	0.300	0.366

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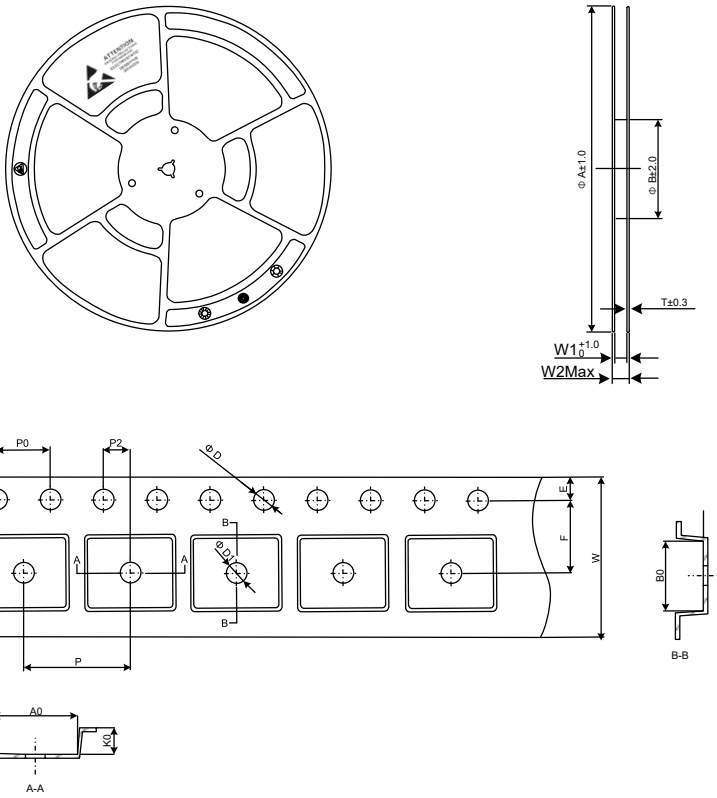
Tape and Reel Information

SOP-7



Reel Dimensions (mm)				
A	**B (Inner Diameter)**	**W1**	**W2 Max**	**T**
330	100	12.4	18.4	1.5

Tape Dimensions			
Symbol	**Dimensions (mm)**	**Symbol**	**Dimensions (mm)**
E	1.75±0.10	W	12.00±0.10
F	5.50±0.10	P	8.00±0.10
P2	2.00±0.10	A0	6.60±0.10
D	$1.50^{+0.1}_{-0}$	B0	5.30±0.10
D1	1.55±0.05	K0	1.90±0.10
P0	4.00±0.10		