Fast Turn-Off, High-Performance Synchronous Rectifier Controller

FEATURES

- **Support DCM, QR and CCM Operation**
- **Integrated with 180V HV Voltage Sense and VDD Supply Circuit, and aux-winding for VDD supply can be eliminated**
- **Integrated with Intelligent Dual LDOs for VDD Supply, SR will work even When Output Voltage Drops Down to Zero**
- **Support Wide Output Range, especially fit for Quick Charger Application with QC, PD Protocol**
- **Support High-Side and Low-Side Configuration**
- **<30ns Fast Turn-Off Delay**
- **Intelligent Turn-on Detection Function**
- **Intelligent ZCD Function**
- **Intelligent Gate Clamp before Start-up**
- **Available with SOT23-6L Package**

APPLICATIONS

- **USB PD Quick Chargers**
- **Adaptors**

GENERAL DESCRIPTION

FC4050LG is a high-performance secondary side synchronous rectifier controller that replaces Schottky diodes in high-efficiency Fly-back converters when combined with an external MOSFET.

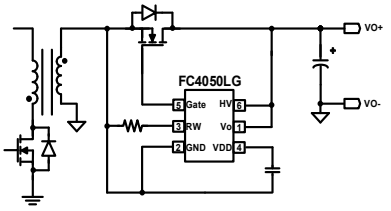
FC4050LG supports High-Side and Low-Side configuration. It also has built-in HV supplies which can eliminate the aux-winding of VDD supply for cost saving.

FC4050LG supports DCM, QR and CCM Operations due to fast turn-off delay of SR MOSFET control.

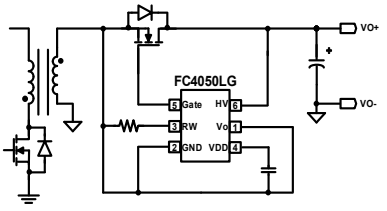
FC4050LG integrates intelligent turn-on detection function which can prevent FC4050LG from turning on falsely due to VDS oscillations at DCM operations.

TYPICAL APPLICATION CIRCUIT

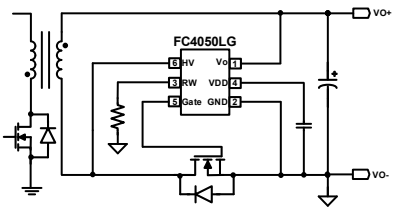
High Side Configuration (VDD=9V)



High Side Configuration (VDD=6V)



Low Side Configuration (VDD=9V)



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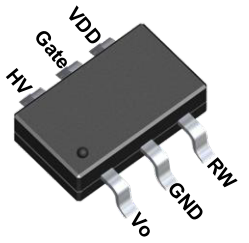
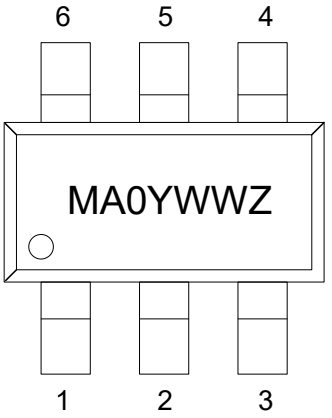
Pin Configuration



SOT23-6

Marking Information



Y：Year Code
WW：Week Code,01-52
Z：Serial Number,0-9 or A-Z

SOT23-6

Pin Description

Pin Number	Pin Name	I / O	Description
1	Vo	I	VDD Power Supply Configuration Pin.
2	GND	P	IC Ground Pin
3	RW	I	Intelligent Turn-on Detection Configuration Pin.
4	VDD	P	IC Power Supply Pin.
5	Gate	O	Gate Drive Output.
6	HV	I	MOSFET Drain Voltage Sense

Ordering Information

Part Number	Description
FC4050LGA	SOT23-6L, Halogen free in T&R, 3000 Pcs/Reel

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Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
HV, Vo Pin Voltage Range	-1 to 180	V
VDD, GATE Pin Voltage Range	-0.3 to 12	V
RW Pin Voltage Range	-0.3 to 5.5	V
VDD DC Clamp Current	5	mA
Package Thermal Resistance----Junction to Ambient (SOT23-6L)	220	°C/W
Package Thermal Resistance----Junction to Case (SOT23-6L)	110	°C/W
Maximum Junction Temperature	150	°C
Storage Temperature Range	-40 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	2.5	kV

Recommended Operation Conditions

Parameter	Value	Unit
Operating Junction Temperature	-40 to 125	°C

Electrical Characteristics (Ta = 25°C, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section (VDD Pin)						
V_{DD_ON}	VDD Under Voltage Lockout Exit			3.8		V
V_{DD_OFF}	VDD Under Voltage Lockout Enter			3.5		V
I_Q	Quiescent Operation Current	VDD=9V			250	μA
V_{DD_reg}	VDD regulation voltage	HV=7V , Vo=0V		6		V
		HV=7V , Vo=12V		9		V
I_{VDD_Max}	VDD maximum charging current	VDD=4V , HV=9V		34		mA
		VDD=7V , Vo=12V		50		mA
I_{op}	Operating current	VDD=9V , CL=2.2nF , fsw = 100kHz		2.2	2.3	mA
		VDD=6V , CL=2.2nF , fsw = 100kHz		1.4	1.5	mA
$V_{o\_LDO\_DIS\_H}$	Vo LDO Disable high threshold voltage			6.7		V

$V_{o\_LDO\_DIS\_L}$	Vo LDO Disable low threshold voltage			6.6		V
External MOSFET Control Section (HV Pin)						
V_{th_off}	SR turn off threshold voltage			0		mV
V_{th_on}	SR turn on threshold voltage	(Note 2)		-220		mV
T_{d_on}	Turn-on delay	CL=2.2nF		25		ns
T_{d_off}	Turn-off delay	CL=2.2nF		22		ns
$T_{d\_off\_pro}$	Turn-off propagation delay			12		ns
LEB	Leading Edge Blanking			1.2		μs
T_{off_min}	Minimum turn-off time			200		ns
Gate Drive						
V_{Gate_L}	Gate Driver low voltage			0	100	mV
V_{Gate_H}	Gate Driver high voltage			VDD		V
I_{Pull_Up}	Gate Driver Maximum Sourcing current			0.8		A
I_{Pull_Down}	Gate Driver Maximum Sinking current			5		A
R_{Pull_Down}	Pull-down impedance				0.4	Ω

Note 1： Exceeding the "limit parameters" in the list may cause permanent damage to the device. The limit parameter is the stress rating. The device may not work properly beyond the recommended operating conditions and stresses, so it is not recommended to let the device work under these conditions. Overexposure to the recommended maximum operating conditions may affect the reliability of the device.

Note 2： The parameters depend on the design and pass the functional test in mass production.

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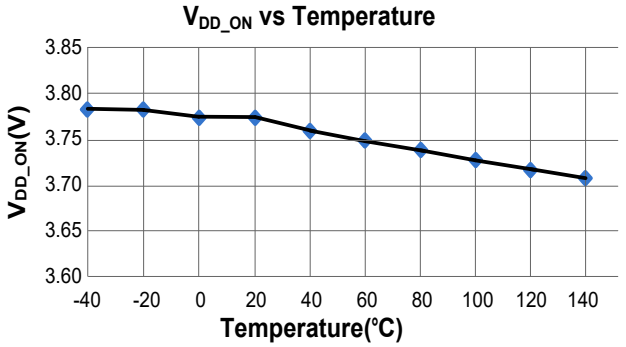
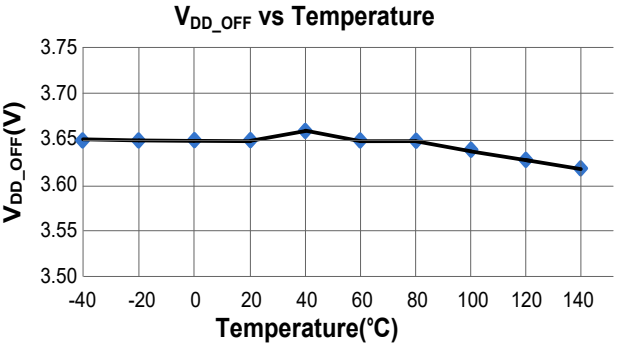
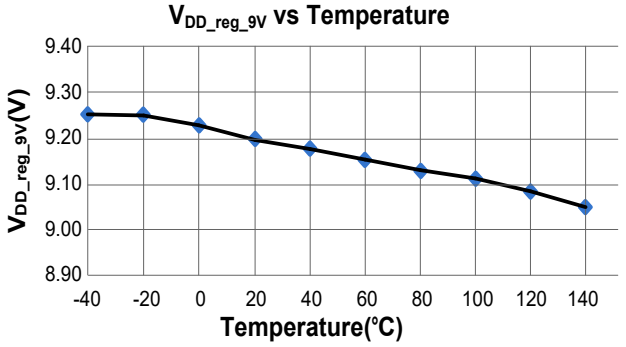
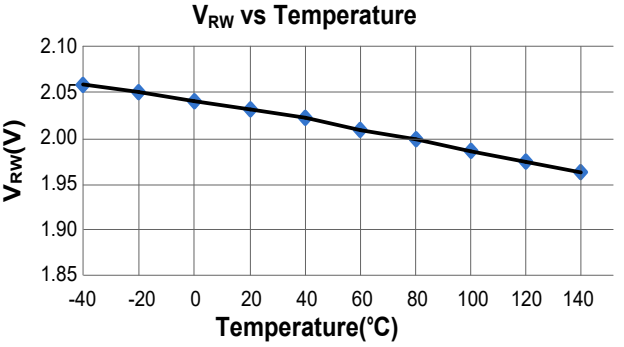
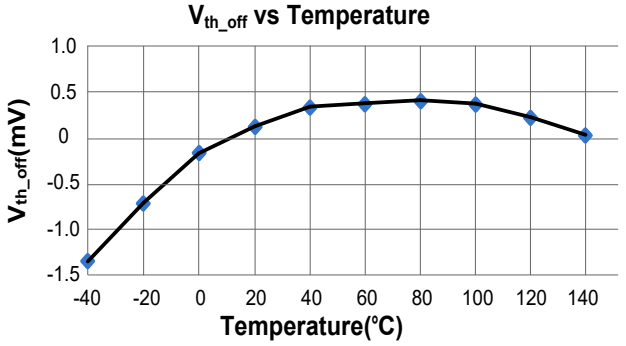
Characterization Plots











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Operation Description

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- **Typical System Implementations**

FC4050LG has dual LDOs for VDD supply. Fig.1 shows the typical low-side configuration. This configuration can support wide range output, and SR MOSFET can work normally even the output drops down to 0V.

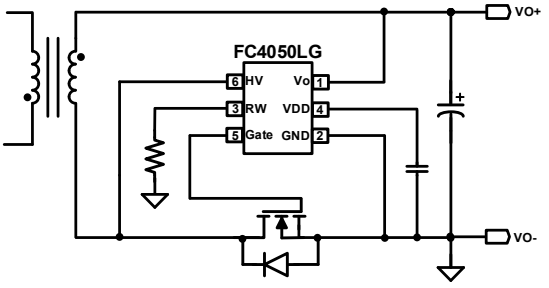

Fig.1

FC4050LG is also used for high-side rectification, there are two types of configuration methods. As shown in Fig.2, Vo pin is connected to HV pin, and VDD is regulated at 9V.

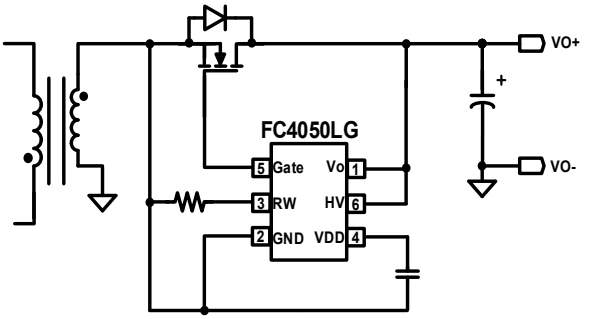

Fig.2

As shown in Fig.3, Vo pin is connected to GND pin, VDD is regulated at 6V.

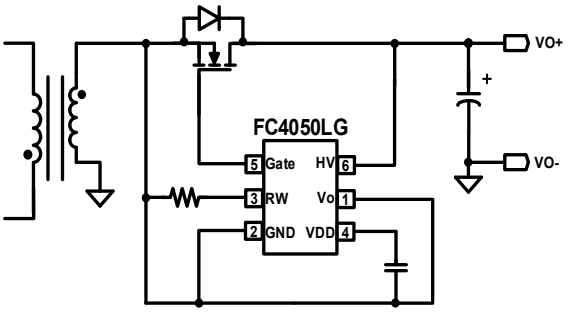

Fig.3

- **System Start-Up Operation**

When VDD pin voltage is below UVLO threshold (3.5V typically), the IC is in sleep mode and the external synchronous MOSFET is kept off. The current flows through body diode of the external synchronous MOSFET. When VDD pin voltage reaches the turn on threshold (3.8V typically), the IC begins working.

- **Turn-on Phase**

At the beginning of the rectification phase, the external synchronous MOSFET is kept off, and the secondary current is conducted through the body diode of the MOSFET. At the same time, a negative Vds voltage (<-500 mV) is formed across the body diode. The negative Vds voltage is much lower than the threshold of the external MOSFET opening detection threshold (-220 mV typically) of FC4050LG, so the external MOSFET is turned on

after the turn-on delay (25 ns typically) (Shown in Fig. 4).

- **Turn-off Phase**

During the conduction phase of the external synchronous MOSFET, FC4050LG senses Vds across the MOSFET. When Vds is higher than the turn-off threshold (0mV typically), the external synchronous MOSFET will be turned off after turn-off delay (22ns typically) (Shown in Fig.4).

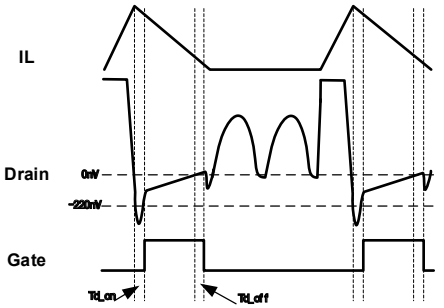

Fig.4

- **Leading Edge Blanking (LEB)**

Each time the external synchronous MOSFET is switched on, a turn-on spike occurs across Vds. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (1.2μs typically), the turn-off comparator is disabled and cannot switch off the external synchronous MOSFET.

- **Intelligent Turn-on Detection Function**

The intelligent turn-on detection function can prevent FC4050LG from turning on falsely due to VDS oscillations at DCM operations, and improve system efficiency and reliability.

- **PCB Layout Guidelines**

PCB design has a significant impact on the performance of synchronous rectification. It is recommended to refer to Figure 5 and Figure 6 when designing synchronous rectification circuit.

1.Make the main power loop Loop1 as small as possible.
2. Make the HV sensing loop Loop3 as small as possible.
3. It is better that Loop1 and Loop3 don't overlap.
4. Make the gate drive loop Loop2 as small as possible.
5. It is recommended to use Ceramic capacitor for VDD supply, and Loop4 should be as small as possible.
6. Keep single-point ground connection between the GND of IC and the source of MOSFET.
7. Figure 6 shows a layout example using PDFN5x6 MOSFET, a transformer and output capacitor. R3 and C2 are the RC snubber network for the SR MOSFET , make the RC loop as small as possible.

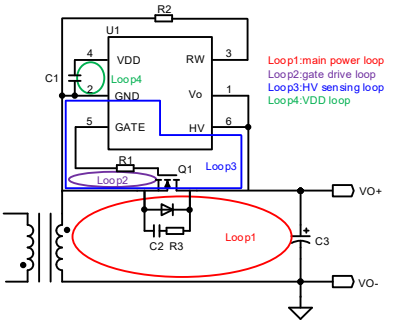

Fig.5

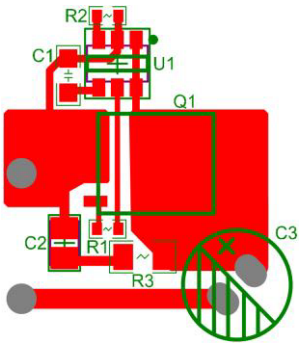

Fig.6

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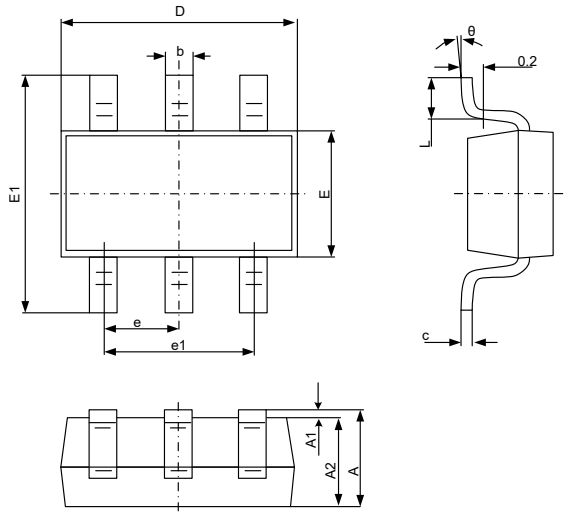
Package Dimension

SOT23-6



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	-	1.350	-	0.053
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.220	0.004	0.009
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°