High-Frequency High-Performance CCM Synchronous Rectifier Switch

FEATURES

- Integrated with 100V 6mΩ MOSFET
- Support Fly-back and Active Clamp Flyback
- Support DCM, QR and CCM Operation
- Integrated with 180V HV Voltage Sense and VDD Supply Circuit, Aux-winding for VDD Supply can be Eliminated
- Support Wide Output Range, Especially Fit for Quick Charger Application with QC, PD Protocol
- Support High-Side and Low -Side Configuration
- <30ns Fast Turn-Off Delay
- Intelligent Turn-on Detection Function
- Intelligent ZCD Function
- Intelligent Gate Clamp before Start-up
- Available with PDFN5*6 Package

GENERAL DESCRIPTION

FC40613 is a high-frequency high-performance CCM synchronous rectifier power switch that can replace Schottky diodes in high-efficiency Fly-back converters using GaN FET.

FC40613 has built-in HV supplies which can eliminate the aux-winding of VDD supply for cost saving, and supports High-Side and Low-Side configuration.

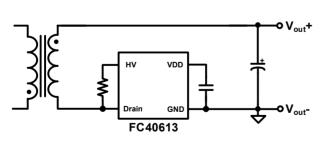
FC40613 can reduce the voltage stress of power device due to fast turn-off of SR MOSFET, thus it can support DCM, QR and CCM operations. FC40613 also integrates with intelligent turn-on detection function which can prevent FC40613 from turning on falsely due to parasitic oscillations.

APPLICATIONS

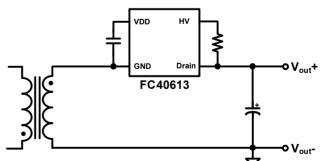
• 30~65W Quick Chargers

TYPICAL APPLICATION CIRCUIT

Low Side configuration



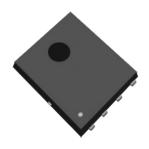
High Side configuration

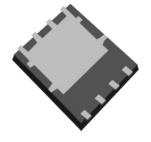


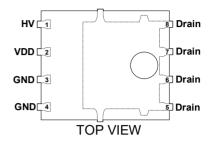


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Pin Configuration







PDFN5*6

Marking Information



XXXXXX: Wafer Lot Code

Y: Year Code

WW: Week Code, 01-52

ZZ: Serial Number, 01-99 or A0-ZZ F: Control Number, 1-9 or A-Z, a-z

PDFN5*6

Typical Output Power Table⁽¹⁾

Product	Dookaga	Recommended Application Range			
	Package	Output Voltage	Output Current		
FC40613	PDFN5*6	3~21V	≤ 5 A		

⁽¹⁾ The Max. output power is limited by junction temperature

Pin Description

Pin Number	Pin Name	Type ⁽²⁾	Description		
1	HV	I	MOSFET drain voltage sense pin. A resistor of $30\sim200\Omega$ (100Ω typically) resistance shall be connected between HV and Drain		
2	VDD	Р	IC power supply pin. A 1μF ceramic chip capacitor is recommended between VDD and GND		
3,4	GND	G	IC Ground Pin		
5,6,7,8	Drain	Р	Drain of Internal MOSFET		

(2) I-Input; P-Power; G-Ground

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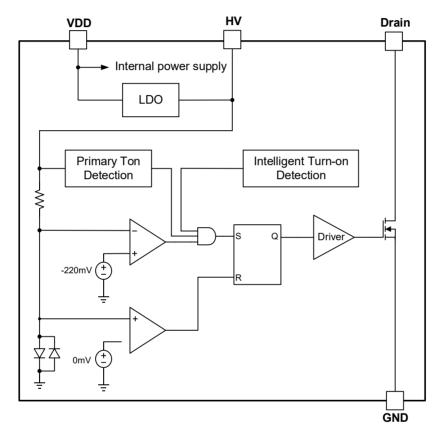
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Ordering Information

Part Number ⁽³⁾	Description			
FC40613QDGA	PDFN5*6, Halogen free in T&R, 5000 Pcs/Reel			

(3) Suffix "A" - Tape & Reel

Block Diagram





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Absolute Maximum Ratings⁽⁴⁾

Parameter	Value	Unit
HV Pin Voltage Range	-1.5 to 180	V
Drain Pin Voltage Range	-1.2 to 100	V
VDD Pin Voltage Range	-0.3 to 12	V
Maximum Junction Temperature	150	°C
Storage Temperature Range	-40 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model) ⁽⁵⁾	2	kV
ESD Capability, CDM (Charge Devices Model) ⁽⁶⁾	2	kV

- (4) Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.
- (5) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (6) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operation Conditions

Parameter	Value	Unit	
Operating Junction Temperature	-40 to 125	Ç	

Electrical Characteristics (VDD=9V, Ta = 25 ℃, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур.	Max	Unit		
Supply Voltage Section (VDD Pin)								
V _{DD_ON}	VDD under voltage lockout exit		3.5	3.8	4.1	V		
V _{DD_OFF}	VDD under voltage lockout enter		3.2	3.5	3.8	V		
lα	Quiescent operation current	HV=0V, VDD=9.6V	220	253	340	μΑ		
V _{DD_reg}	VDD regulation voltage	HV=10V	5.6	6	6.4	٧		
I _{op}	Operating current	fsw = 50kHz , VDD=9V	0.6	1.7	4	mA		
IVDD_Max	VDD Maximum charging current	VDD=4V , HV=40V	25	34	55	mA		



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Control Sec	tion (HV Pin)					
V _{th_off}	SR turn off threshold voltage ⁽⁷⁾			0		mV
V _{th_on}	SR turn on threshold voltage ⁽⁷⁾			-220		mV
T _{d_on}	Turn-on delay ⁽⁷⁾			25		ns
T_{d_off}	Turn-off delay ⁽⁷⁾			22		ns
T _{LEB}	Leading edge blanking ⁽⁷⁾			490		ns
$T_{\text{off_min}}$	Minimum turn-off time ⁽⁷⁾			200		ns
Internal MO	SFET					•
V_{BR}	Internal MOSFET drain- source breakdown voltage		100	108		V
I _{D_Pulse}	Internal MOSFET maximum pulse drain current				210	Α
I _D	Internal MOSFET maximum continuous drain current				93	А
D.	Internal MOSFET drain- source on-state resistance	V _{GS} =10V , I _D =20A		6	7.6	mΩ
R_{ds_on}		V _{GS} =4.5V , I _D =15A		8	10	mΩ

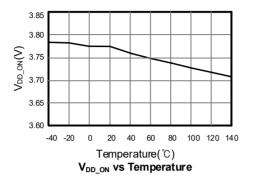
⁽⁷⁾ Guaranteed by the design and pass the functional test in mass production.

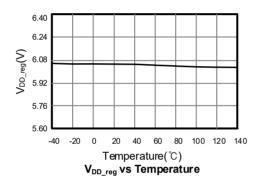
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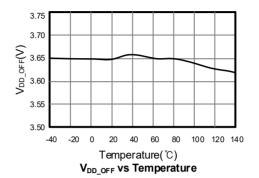


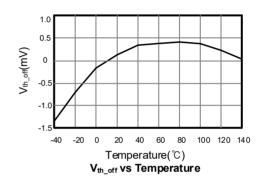
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Characterization Plots











High-Frequency High-Performance CCM Synchronous Rectifier Switch Operation Description

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ON/OFF of the IC

Before VDD pin voltage rises to turn on threshold V_{DD_ON} (3.8V typically), FC40613 remains OFF state. Intelligent gate clamp circuit inside can prevent IC from turning on falsely due to dv/dt of drain voltage. When VDD pin voltage reaches V_{DD_ON} , the IC changes to ON state and begins working, the current flows through channel of the internal MOSFET. When VDD pin voltage is below UVLO threshold V_{DD_OFF} (3.5V typically), the IC goes back to OFF state and the current flows through body diode of the internal MOSFET.

Turn-on Phase

At the beginning of the rectification phase, the channel of internal synchronous MOSFET is kept off, and the secondary current is conducted through the body diode of the MOSFET. At the same time, a negative Vds voltage (<-500 mV) is formed across the body diode. When negative Vds voltage is lower than the threshold of the internal MOSFET opening detection threshold V_{th_on} (-220 mV typically), the channel of the internal MOSFET is turned on after the turn-on delay T_{d_on} (25 ns typically) (Shown in Fig. 1).

Turn-off Phase

During the conduction phase of the internal SR MOSFET, FC40613 senses Vds across the MOSFET. When Vds is higher than the turn-off threshold V_{th_off} (0mV typically), the channel of the internal synchronous MOSFET will be turned off after turn-off delay T_{d_off} (22ns typically) (Shown in Fig.1).

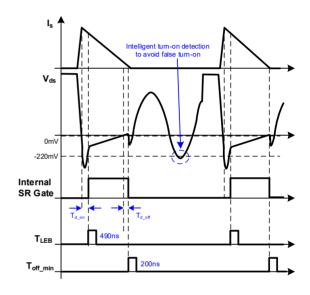


Fig.1

Leading Edge Blanking (LEB)

Each time the internal SR MOSFET is switched on, a turn-on spike occurs across Vds. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period T_{LEB} (490ns typically), the turn-off comparator is disabled and cannot switch off the internal SR MOSFET. After T_{LEB} ends, the turn-off comparator is enable (Shown in Fig.1).

Minimum Off Time

Each time the internal SR MOSFET is switched off, turn-off spike may occur across Vds. To avoid false turn-on of SR MOSFET, a period of minimum off time is inserted. During minimum off time Toff_min

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FC40613QDGA

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(200ns typically), the turn-on comparator is disabled and cannot switch on the internal SR MOSFET. After $T_{\text{off_min}}$ ends, the turn-on comparator is enable (Shown in Fig.1).

• Intelligent Turn-on Detection Function

The intelligent turn-on detection function can prevent FC40613 from turning on falsely due to parasitic oscillations, and improve system efficiency and reliability (Shown in Fig.1).

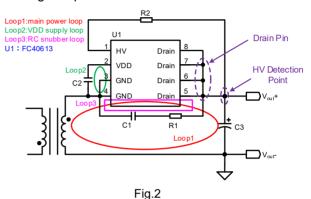
Application Information

PCB Layout Guidelines

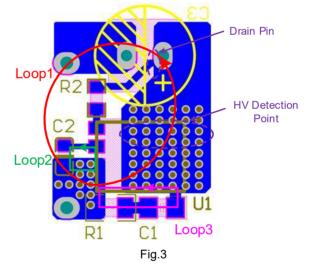
PCB design has a significant impact on the performance of synchronous rectification. It is recommended to refer to Fig.2 and Fig.3 when designing SR circuit.

- 1. Make the main power loop Loop1 as small as possible.
- It is recommended to use ceramic chip capacitor for VDD supply (1µF typically), and Loop2 should be as small as possible.
- 3. A resistor of 30~200Ω (100Ω typically) resistance shall be connected between HV and Drain. The position of HV detection point has an impact on the CCM Voltage stress. The farther the HV detection point is from the Drain pin, the smaller the CCM voltage Stress. In the high side configuration shown in Fig.3, it is recommended that HV be connected to the positive side of the output capacitor through the R2 resistor.
- 4. R1 and C1 are the RC snubber network for the

- SR MOSFET, make the RC loop Loop3 as small as possible.
- Fig.3 shows a layout example using FC40613, a transformer and output capacitor. Make the PCB heat dissipation area of the drain pin as large as possible.



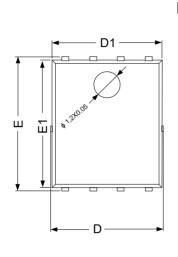
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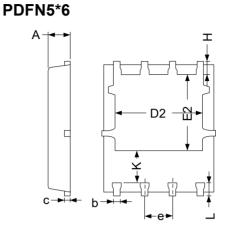


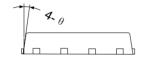


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Package Dimension







Or made al	Dimensions in Millimeters			Dimensions in Inches			
Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	
А	0.950	1.000	1.050	0.037	0.039	0.041	
b	0.250	0.300	0.350	0.010	0.012	0.014	
С	0.200	0.250	0.300	0.008	0.010	0.012	
D		5.150 (BSC)			0.203 (BSC)		
D1	4.900	5.000	5.100	0.193	0.197	0.201	
D2	3.900	4.010	4.200	0.154	0.158	0.165	
Е		6.150 (BSC)		0.242 (BSC)			
E1	5.750	5.850	5.950	0.226	0.230	0.234	
E2	3.350	3.500	3.650	0.132	0.138	0.144	
е	1.170	1.270	1.370	0.046	0.050	0.054	
Н	0.510	0.610	0.710	0.020	0.024	0.028	
L	0.510	0.610	0.710	0.020	0.024	0.028	
θ	9°	11°	13°	9°	11°	13°	
K	1.100	1.350	1.500	0.043	0.053	0.059	

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