60V, 1.2A, 480kHz Non-synchronous Buck Converter

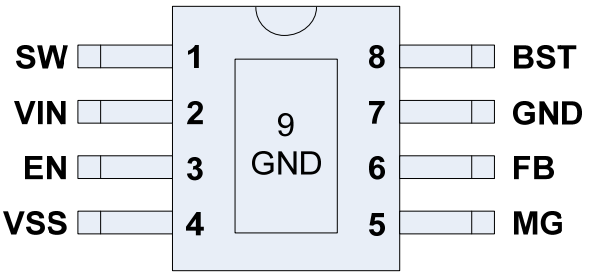
General Description

The FTD1670 is a monolithic, step-down, switch mode converter with a built-in power MOSFET. It achieves a 1.2A peak-output current over input supply 10V-60V with excellent load and line regulation. Current-mode operation provides a fast transient response and eases loop stabilization. Fault condition protections include cycle-by-cycle current limiting and thermal shutdown.
The FTD1670 requires a minimal number of readily-available external components.
The FTD1670 is available in a ESOP-8 package.

Features

- 1.2A Peak Output Current
- 0.7Ω Internal Power MOSFET
- Stable with Low-ESR Ceramic Output Capacitors
- Up to 91% Efficiency
- 0.1μA Shutdown Mode
- Fixed 480kHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over-Current Protection
- 11V to 60V Operating Input Range
- Max duty 90%
- Available in a ESOP-8 Package

Pin Configurations



(Top view)

Applications

- Power Meters
- Distributed Power Systems
- Battery Chargers
- Pre-Regulator for Linear Regulators
- WLED Drivers

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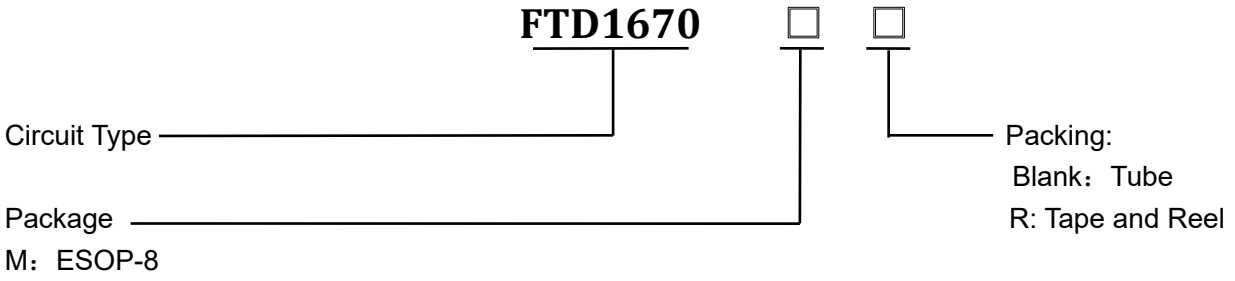
Pin Description

Pin Number	Pin Name	Description
1	SW	Power Switching Output. It is the Drain of the N-Channel power MOSFET to supply power to the output LC filter.
2	VIN	Supply Voltage. The FTD1670 operates from a 10V-to-60V unregulated input. Requires C1 to prevent large voltage spikes from appearing at the input.
3	EN	On/Off. Pull EN above 1.35V to turn the device ON. For automatic enable, connect to V_{IN} using a 1MΩ resistor.
4	VSS	Source of the MOS
5	MG	Gate of the MOS
6	FB	Feedback. Sets the output voltage. Connect to the tap of an external resistor divider from the output to GND. The frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 300mV to prevent current-limit runaway during a short-circuit fault.
7	BST	Bootstrap. Connect a capacitor between the SW and BS pins to form a floating supply across the power switch driver. This capacitor drives the power switch's gate above the supply voltage.
8	GND	Ground. Voltage reference for the regulated output voltage. Requires special layout considerations. Isolate this node from the D1 to C1 ground path to prevent switching current spikes from inducing.

Ordering Information



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Function Block

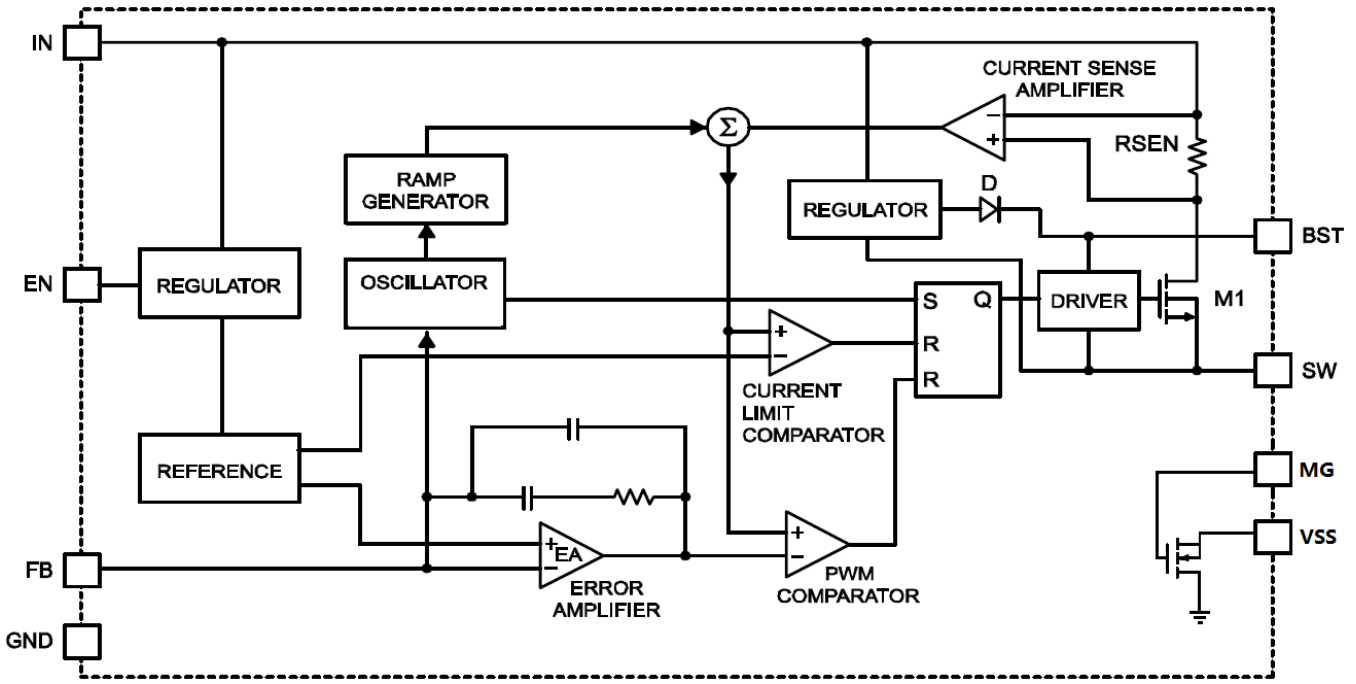

Figure1 Function Block Diagram of FTD1670

Absolute Maximum Ratings (Note1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Supply Voltage（VIN to Gnd）	-0.3 ~ 60	V
V_{SW}	SW to GND Voltage	-0.3 to V_{IN}+0.3	V
V_{BS}	BS to GND Voltage	V_{SW} - 0.3 ~ V_{SW} +6	V
	All Other Pins	-0.3 ~ 6	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	150	℃
T_{STG}	Storage Temperature	-65 ~ 150	℃
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	℃

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	60	℃/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operation Conditions (Note3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	11 ~ 60	V
V_{OUT}	Converter Output Voltage	V_{FB} ~ V_{IN}*90%	V
	Operating Junction Temp	-40 ~ 125	℃

Note 3: Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=12V, V_{EN}=3V and T_A = 25℃

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{FB}	Feedback Voltage	10V ≤ V_{IN} ≤ 60V	0.792	0.812	0.832	V
I_{FB}	Feedback Current	VFB = 0.85V	-	-	0.1	μA
$R_{DS(ON)}$	Switch-On Resistance		-	0.7	-	Ω
I_{SW_LKG}	Switch Leakage	V_{EN}=0V,V_{SW}=0V	-	-	1	μA
I_{LIM}	Current Limit		-	1.65	-	A
f_{SW}	Oscillator Frequency	V_{FB}=0.6V	380	480	580	kH_Z
f_{SW_F}	Foldback Frequency	V_{FB}=0V	-	120	-	KH_Z
D_{MAX}	Maximum Duty Cycle	V_{FB}=0.6V	-	90	-	%
T_{ON}	Minimum ON-Time		-	100	-	ns
V_{UVLO_R}	Under-Voltage Lockout Threshold, Rising		-	7.5	8.5	V
V_{UVLO_F}	Under-Voltage Lockout Threshold, Falling		-	7.1	-	V
V_{UVLO_HYS}	Under-Voltage Lockout Threshold,Hysteresis		-	0.4	-	V
V_{EN_R}	EN Threshold, Rising		-	1.35	-	V

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V_{EN_F}	EN Threshold, Falling		-	1.17	-	V
V_{EN_HYS}	EN Threshold, Hysteresis		-	180	-	mv
I_{EN}	EN Input Current	VEN=2V	-	3.1	-	μA
		VEN=0V	-	0.1	-	μA
I_S	Supply Current (Shutdown)	VEN=0V	-	0.1	1	μA
I_Q	Supply Current (Quiescent)	VEN=2V,VFB=1V	-	0.73	0.85	mA
T_{SD}	Thermal Shutdown		-	165	-	℃
T_{SD_HYS}	Thermal Shutdown Hysteresis		-	20	-	℃

(Hotswap FET)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250μA	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS}=0V	-	-	1	μA
		T_J=85℃	-	-	30	
I_D	Continue Drain Current	-	-	-	3	A
$R_{DS(ON)}$	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=0.5A	-	225	325	mΩ
		V_{GS}=4.5V, I_{DS}=0.5A	-	280	350	
V_{GSS}	Gate-Source Breakdown Voltage	-	20	-	-	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250μA	1	1.8	2.5	V
V_{SD}	Diode Forward Voltage	I_{DS}=0.5A, V_{GS}=0V	-	0.7	1.3	V

OPERATION

The FTD1670 is a current mode buck regulator. That is, the EA output voltage is proportional to the peak inductor current.

At the beginning of a cycle, M1 is off. The EA output voltage is higher than the current sense amplifier output, and the current comparator's output is low. The rising edge of the 480kHz CLK signal sets the RS Flip-Flop. Its output turns on M1 thus connecting the SW pin and inductor to the input supply.

The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is summed to the Current Sense Amplifier output and compared to the Error Amplifier output by the PWM Comparator. When the sum of the Current Sense Amplifier output and the Slope Compensation signal exceeds the EA output voltage, the RS Flip-Flop is reset and M1 is turned off. The external Schottky rectifier diode (D1) conducts the inductor current.

If the sum of the Current Sense Amplifier output and the Slope Compensation signal does not exceed the EA output for a whole cycle, then the falling edge of the CLK resets the Flip-Flop.

The output of the Error Amplifier integrates the voltage difference between the feedback and the 0.812V bandgap reference. The polarity is such that lower than 0.812V FB pin voltage increases the EA output voltage. Since the EA output voltage is proportional to the peak inductor current, an increase in its voltage also increases current delivered to the output.

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Application Information

Setting Output Voltage

The external resistor divider sets the output voltage (see the Typical Application schematic). Table 1 lists resistors for common output voltages. The feedback resistor (R2) also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). R1 is:

$$R1 = \frac{R2}{\frac{V_{OUT}}{0.812V} - 1}$$

Table 1:Resistor Selection for Common output voltages

VOUT(V)	R1(KΩ)	R2(KΩ)
1.8	102(1%)	124(1%)
2.5	59(1%)	124(1%)
3.3	40.2(1%)	124(1%)
5	23.7(1%)	124(1%)

Selecting the Inductor

Use an inductor with a DC current rating at least 25% percent higher than the maximum load current for most applications. For best efficiency, the inductor's DC resistance should be less than 200mΩ.

For most designs, the required inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}}$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use a larger inductance to improve efficiency.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high-frequency-switching current from passing through the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESRs and small temperature coefficients. For most applications, a 4.7μF capacitor will sufficient.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance should be low at the switching frequency. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR characteristics. For most applications, a 22μF ceramic capacitor will sufficient.

PCB Layout Guide

PCB layout is very important to stability. Please follow these guidelines and use Figure 2 as reference.

1) Keep the path of switching current short and minimize the loop area formed by the input capacitor, high-side MOSFET, and Schottky diode.

2) Keep the connection from the power ground→Schottky diode→SW pin as short and wide as possible.

3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.

4) Route SW away from sensitive analog areas such as FB.

5) Connect IN, SW, and especially GND to large copper areas to cool the chip for improved thermal performance and long- term reliability. For single layer PCBs, avoid soldering the exposed pad.

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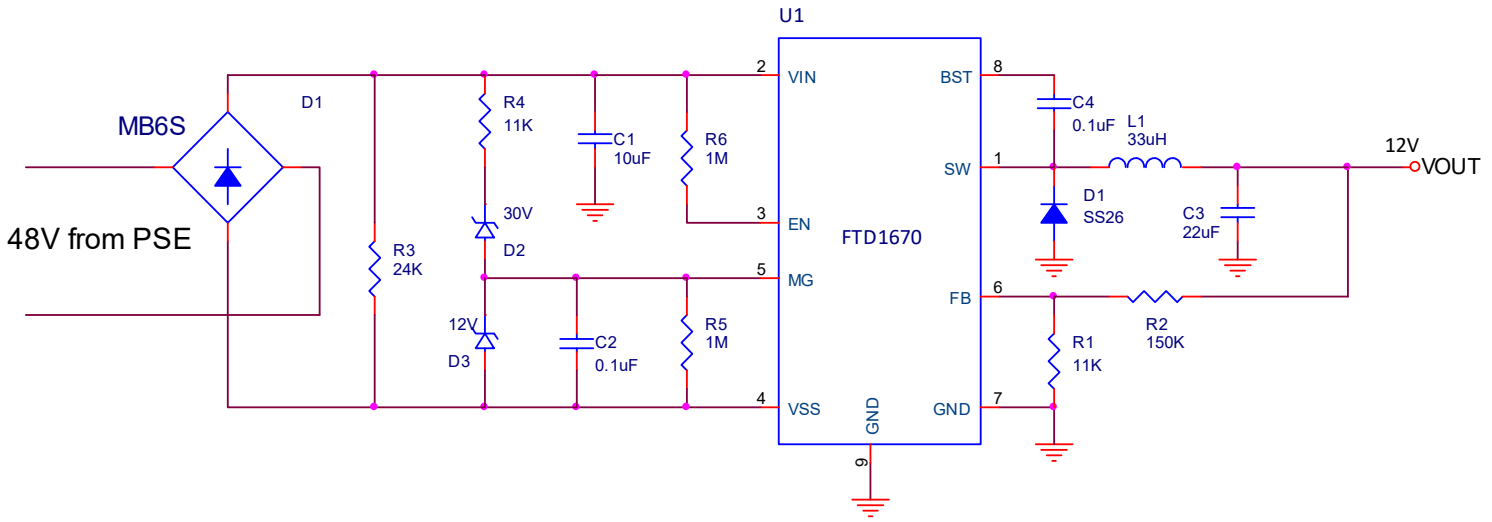
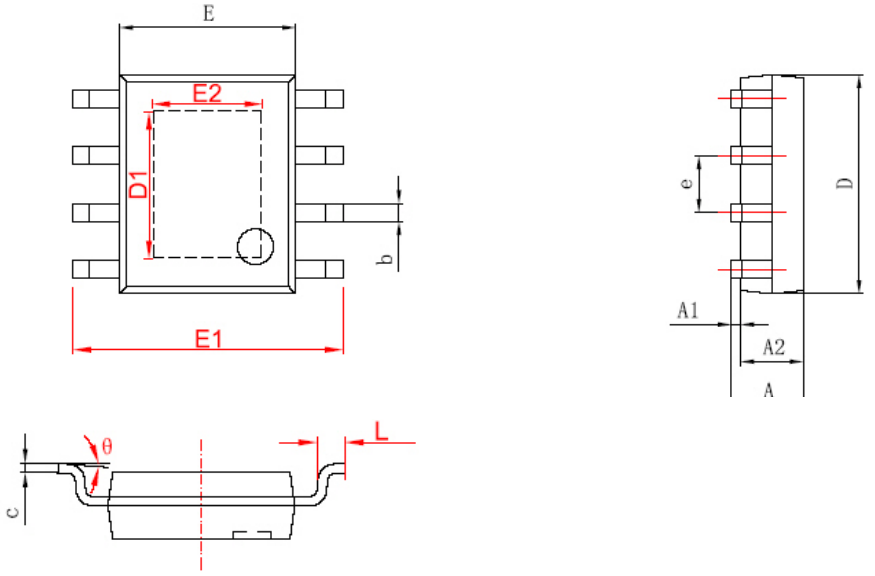
Typical Application Circuit



Package information

ESOP-8 Package Outline Dimensions



	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°