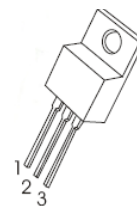


TIP120,121,122 Darlington TRANSISTOR (NPN)

TIP125,126,127 Darlington TRANSISTOR (PNP)

TO-220

1.BASE
2.COLLECTOR
3.EMITTER



FEATURES

Medium Power Complementary silicon transistors

MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Symbol	Parameter	TIP120	TIP121	TIP122	Units
		TIP125	TIP126	TIP127	
V _{CBO}	Collector-Base Voltage	60	80	100	V
V _{CEO}	Collector-Emitter Voltage	60	80	100	V
V _{EBO}	Emitter-Base Voltage	5			V
I _C	Collector Current -Continuous	5			A
P _C	Collector Power Dissipation	2			W
R _{θJA}	Thermal Resistance Junction to Ambient	62.5			°C/W
R _{θJc}	Thermal Resistance Junction to Case	1.92			°C/W
T _J	Junction Temperature	150			°C
T _{stg}	Storage Temperature	-55to+150			°C

ELECTRICAL CHARACTERISTICS (T_{amb}=25°C unless otherwise specified)

Parameter	Symbol	Test conditions	MIN	MAX	UNIT
Collector-base breakdown voltage TIP120,TIP125 TIP121,TIP126 TIP122,TIP127	V(BR) _{CBO}	I _C = 1mA, I _E =0	60 80 100		V
Collector-emitter breakdown voltage TIP120,TIP125 TIP121,TIP126 TIP122,TIP127	V _{CEO(SUS)}	I _C = 30mA, I _B =0	60 80 100		V
Collector cut-off current TIP120,TIP125 TIP121,TIP126 TIP122,TIP127	I _{CBO}	V _{CB} = 60 V, I _E =0 V _{CB} = 80 V, I _E =0 V _{CB} = 100V, I _E =0		0.2	mA
Collector cut-off current TIP120,TIP125 TIP121,TIP126 TIP122,TIP127	I _{CEO}	V _{CE} =30 V, I _B =0 V _{CE} =40 V, I _B =0 V _{CE} =50 V, I _B =0		0.5	mA
Emitter cut-off current	I _{EBO}	V _{EB} =5 V, I _C =0		2	mA
DC current gain	h _{FE(1)}	V _{CE} = 3V, I _C =0.5A	1000		
	h _{FE(2)}	V _{CE} = 3V, I _C =3 A	1000		
Collector-emitter saturation voltage	V _{CE(sat)}	I _C =3A, I _B =12mA I _C =5 A, I _B =20mA		2 4	V
Base-emitter voltage	V _{BE}	V _{CE} =3V, I _C =3 A		2.5	V
Output Capacitance TIP125,TIP126,TIP127 TIP120,TIP121,TIP122	C _{ob}	V _{CB} =10V, I _E =0, f=0.1MHz		300 200	pF

Typical Characteristics

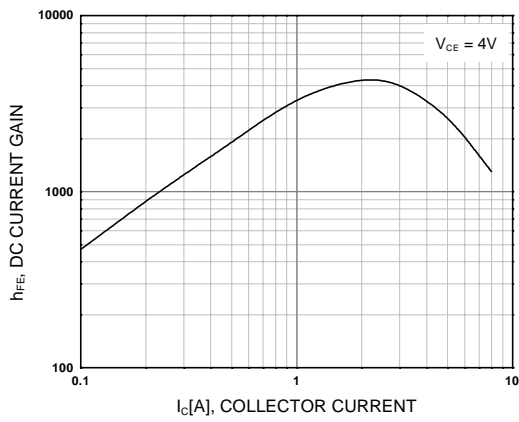


Figure 1. DC current Gain

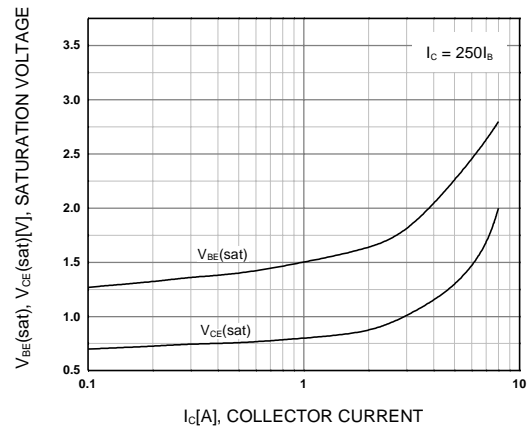


Figure 2. Base-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage

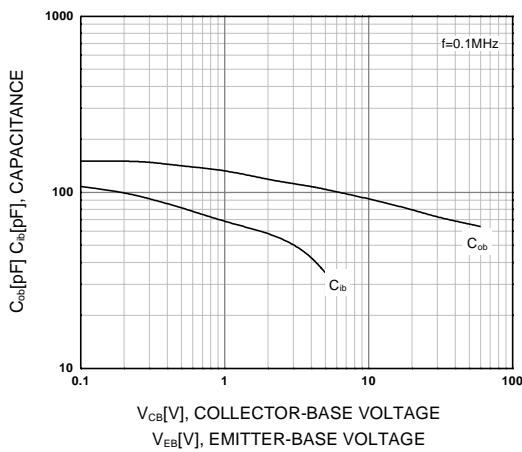


Figure 3. Output and Input Capacitance
vs. Reverse Voltage

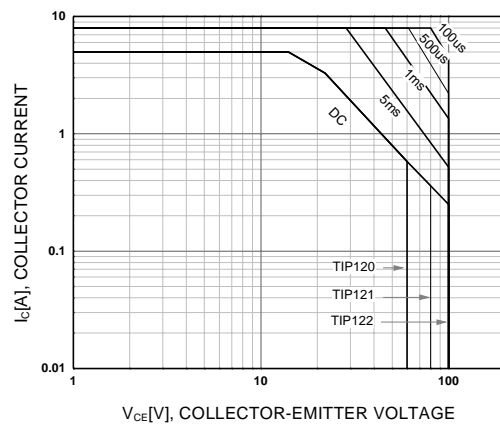


Figure 4. Safe Operating Area

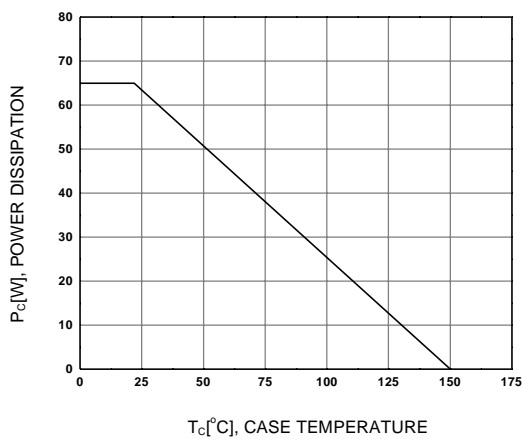


Figure 5. Power Derating