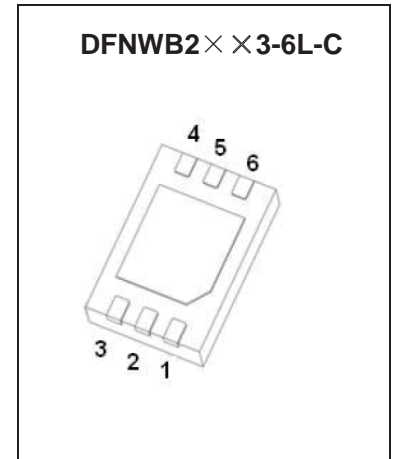


Dual N-Channel MOSFET

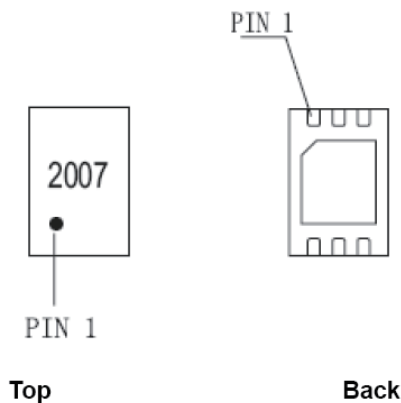
$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
20V	20mΩ@10V	7A
	22mΩ@4.5V	
	24mΩ@3.8V	
	26mΩ@2.5V	
	35mΩ@1.8V	



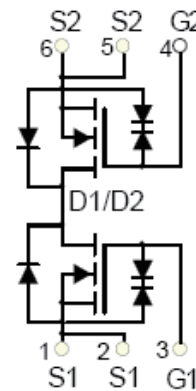
DESCRIPTION

The FTK2007DFN23 uses advanced trench technology to provide excellent $R_{DS(ON)}$ low gate charge. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch, facilitated by its common-drain configuration.

MARKING:



Equivalent Circuit



MAXIMUM RATINGS ($T_a=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current	I_D	7	A
Pulsed Drain Current	I_{DM}^*	30	A
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	125	$^{\circ}C/W$
Junction Temperature	T_j	150	$^{\circ}C$
Storage Temperature	T_{stg}	-55~+150	$^{\circ}C$
Lead Temperature for Soldering Purposes(1/8" from case for 10 s)	T_L	260	$^{\circ}C$

*Repetitive rating: Pulse width limited by junction temperature.



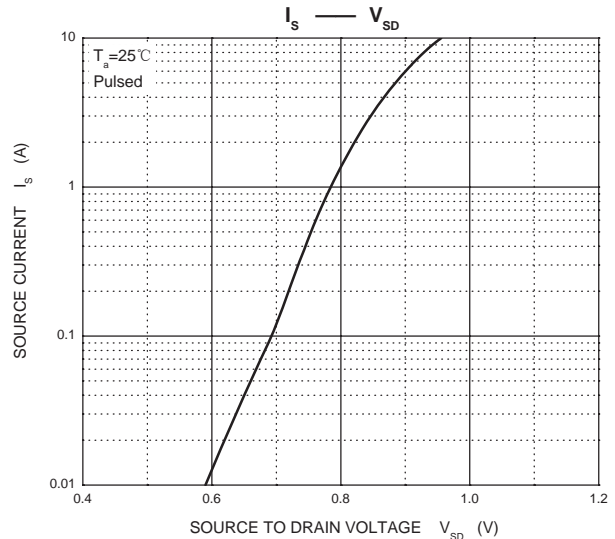
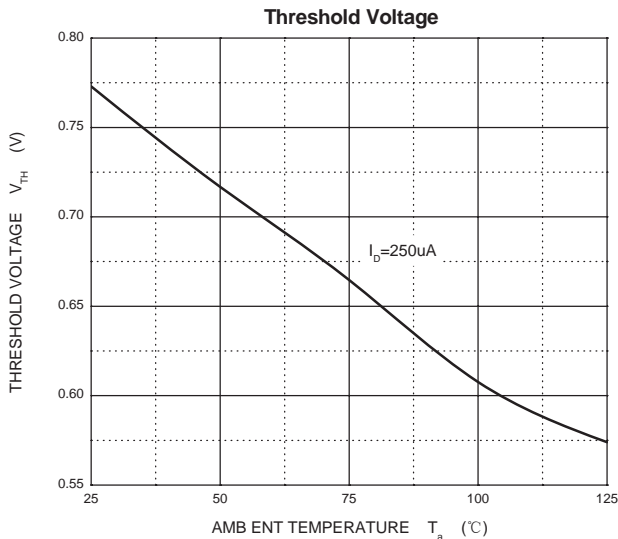
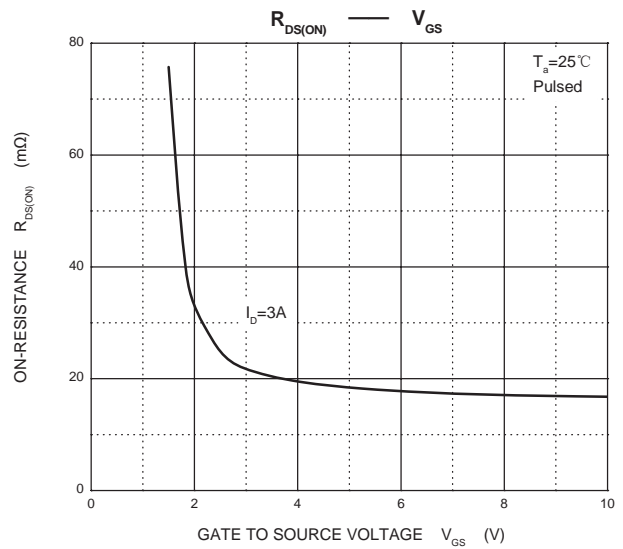
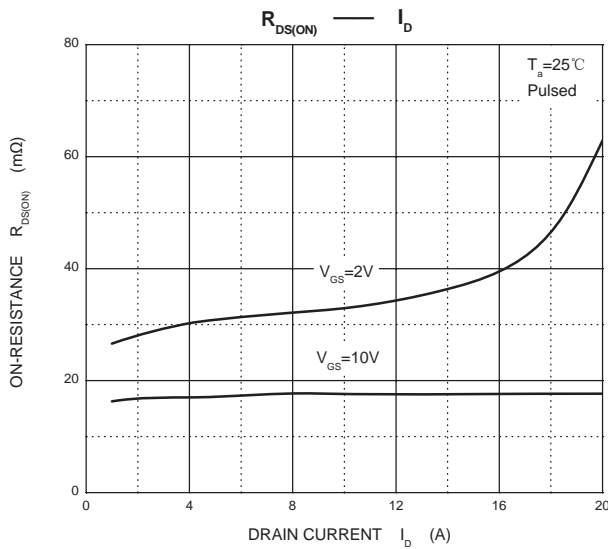
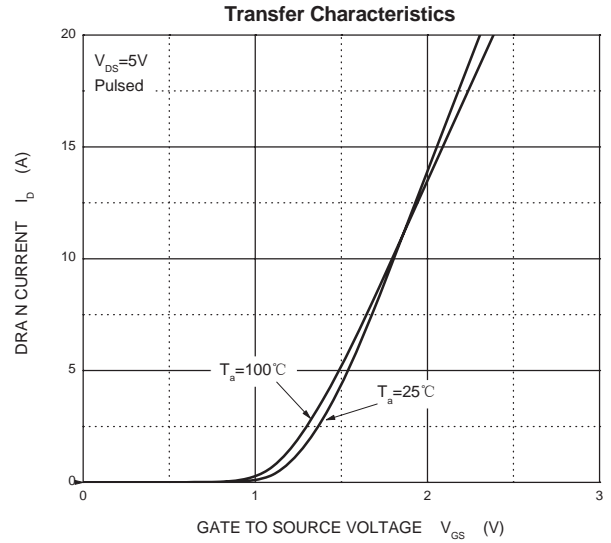
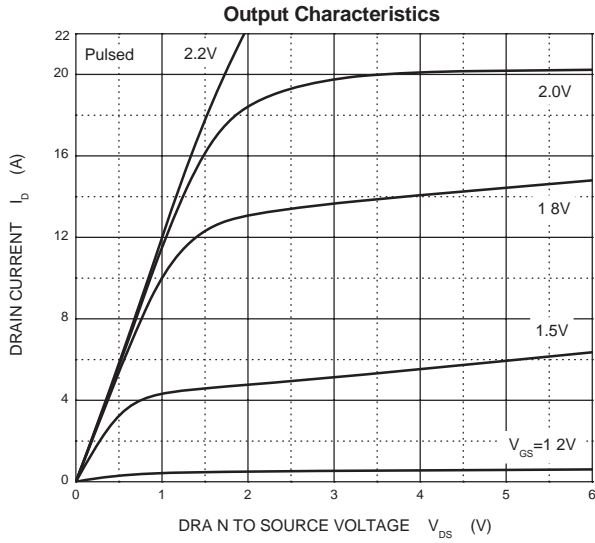
Electrical characteristics (T_a=25 unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
STATIC PARAMETERS							
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	20			V	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 16V, V _{GS} = 0V			1	μA	
Gate-body leakage current	I _{GSS}	V _{GS} = ±4.5V, V _{DS} = 0V			±1	μA	
		V _{GS} = ±8V, V _{DS} = 0V			±10	μA	
Gate threshold voltage (note 1)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	0.4		1	V	
Drain-source on-resistance (note 1)	R _{DS(on)}	V _{GS} = 10V, I _D = 7A			20	mΩ	
		V _{GS} = 4.5V, I _D = 6.6A			22	mΩ	
		V _{GS} = 3.8V, I _D = 6A			24	mΩ	
		V _{GS} = 2.5V, I _D = 5.5A			26	mΩ	
		V _{GS} = 1.8V, I _D = 5A			35	mΩ	
Forward tranconductance (note 1)	g _{FS}	V _{DS} = 5V, I _D = 7A	9			S	
Diode forward voltage(note 1)	V _{SD}	I _S = 1A, V _{GS} = 0V			1	V	
DYNAMIC PARAMETERS (note 2)							
Input Capacitance	C _{iss}	V _{DS} = 10V, V _{GS} = 0V, f = 1MHz		1150		pF	
Output Capacitance	C _{oss}				185		pF
Reverse Transfer Capacitance	C _{rss}				145		pF
Total gate charge	Q _g	V _{DS} = 10V, V _{GS} = 4.5V, I _D = 7A		15		nC	
Gate-source charge	Q _{gs}				0.8		nC
Gate-drain charge	Q _{gd}				3.2		nC
SWITCHING PARAMETERS (note 2)							
Turn-on delay time	t _{d(on)}	V _{GS} = 5V, V _{DD} = 10V, R _L = 1.35Ω, R _{GEN} = 3Ω		6		ns	
Turn-on rise time	t _r				13		ns
Turn-off delay time	t _{d(off)}				52		ns
Turn-off fall time	t _f				16		ns

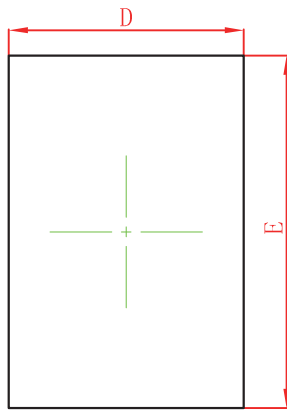
Notes :

1. Pulse Test : Pulse width ≤ 300μs, duty cycle ≤ 0.5%.
2. Guaranteed by design, not subject to production testing.

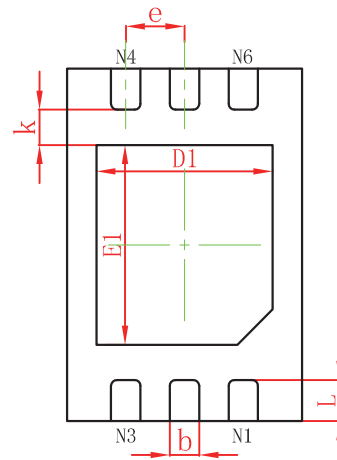
Typical Characteristics



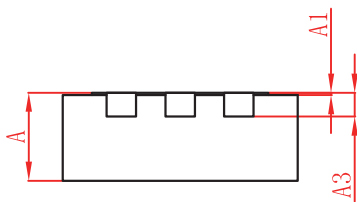
DFNWB2 × 3-6L Package Outline Dimensions(Unit:mm)



TOP VIEW



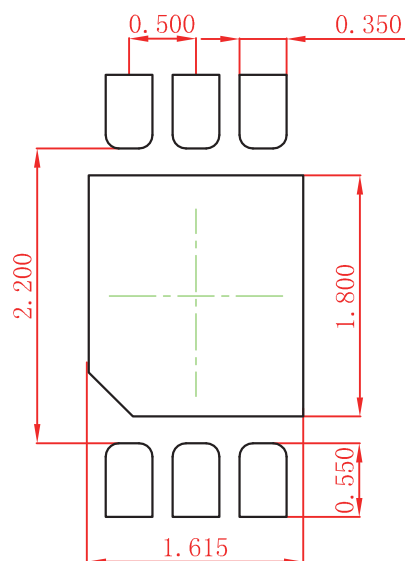
BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.950	2.050	0.077	0.081
E	2.950	3.050	0.116	0.120
D1	1.450	1.550	0.057	0.061
E1	1.650	1.750	0.065	0.069
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.300	0.400	0.012	0.016

DFNWB2 × 3-6L Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.050\text{mm}$.
3. The pad layout is for reference purposes only.