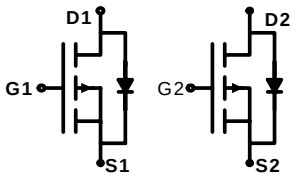
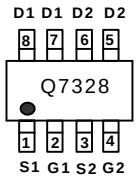
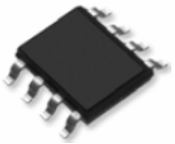
Dual P-Channel MOSFET



Schematic diagram



Marking and pin Assignment


SOP-8 top view

DESCRIPTION

The FTK7328 uses advanced processing techniques to achieve extremely low on-resistance. This benefit, combined with the ruggedized device design that the MOSFETs are well know for. provides the designer with an extremely efficient and reliable device for use in battery and load management.

FEATURES

Ultra Low On-Resistance

Maximum ratings (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	
Continuous Drain Current	I_D	-8	A
Pulsed Drain Current (note 1)	I_{DM}	-32	
Power Dissipation (note 2)	P_D	1.4	W
Thermal Resistance from Junction to Ambient (note 2)	$R_{\theta JA}$	89	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{stg}	-55 ~+150	

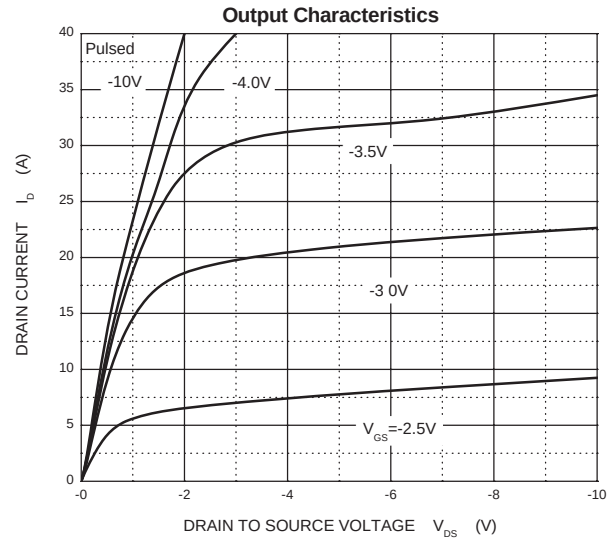
Electrical characteristics (T_a=25℃ unless otherwise noted)

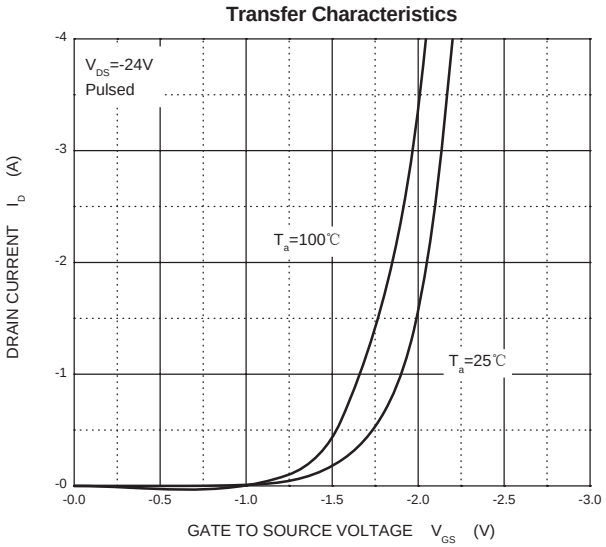
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V, V_{GS}=0V			-15	μA
Gate body Leakage	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-1		-2.5	V
Drain-Source on-state Resistance (note 3)	$R_{DS(on)}$	V_{GS} =-10V, I_D =-8A			21	mΩ
		V_{GS} =-4.5V, I_D =-6.8A			32	
Forward Transconductance	g_{Fs}	V_{DS} =-10V, I_D =-8A	12			S
Dynamic Characteristics (note 4)						
Input Capacitance	C_{iss}	V_{DS} =-25V,V_{GS} =0V,f =1MHz		2675		pF
Output Capacitance	C_{oss}			409		
Reverse Transfer Capacitance	C_{rss}			262		
Total Gate Charge	Q_g	V_{DS} =-15V,V_{GS} =-10V,I_D =-8A			78	nC
Gate-Source Charge	Q_{gs}			9.8		
Gate-Drain Charge	Q_{gd}			8.3		
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=-15V,R_D=15Ω I_D =-1A,V_{GS}=-10V,R_G=6Ω			20	ns
Rise Time	t_r				23	
Turn-Off Delay Time	$t_{d(off)}$				297	
Fall Time	t_f				147	
Drain-Source Body Diode Characteristics						
Diode Forward Voltage (note 3)	V_{SD}	I_S=-2A,V_{GS}=0V			-1.2	V

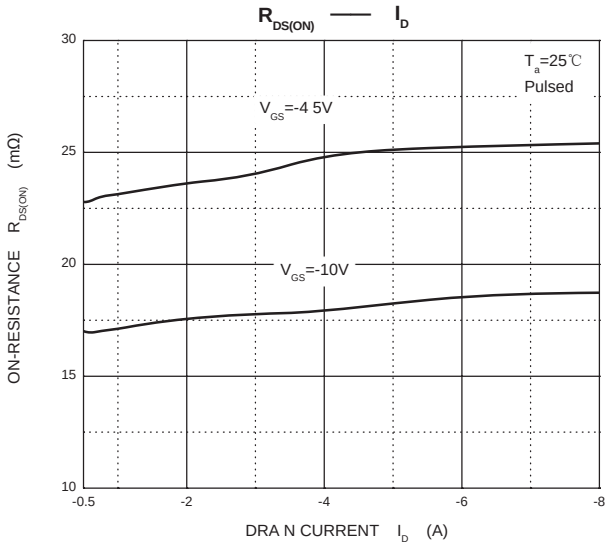
Notes:

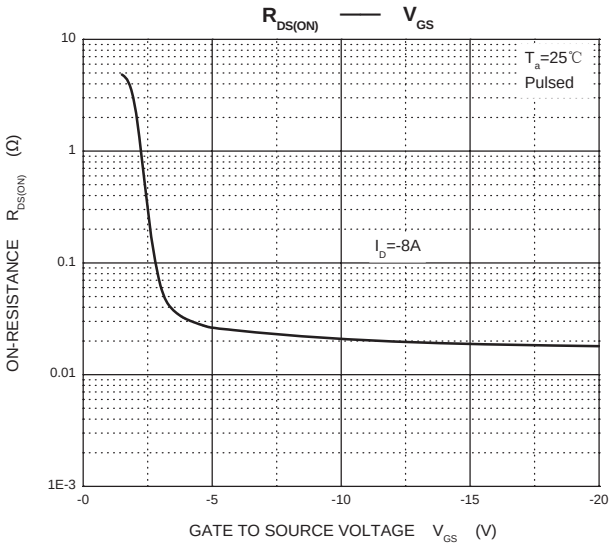
1. Repetitive rating : Pulse width limited by junction temperature.
2. Surface mounted on 1”×1” FR4 board,t≤10s.
3. Pulse Test : Pulse Width≤300μs, Duty Cycle ≤2%.
4. Guaranteed by design, not subject to production testing.

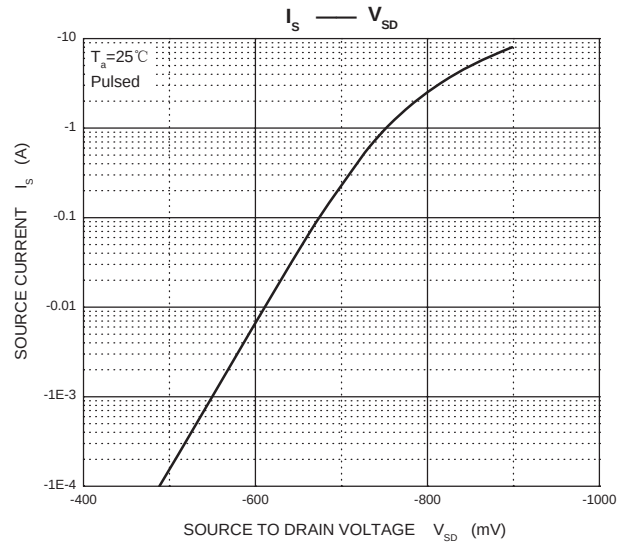
Typical Characteristics

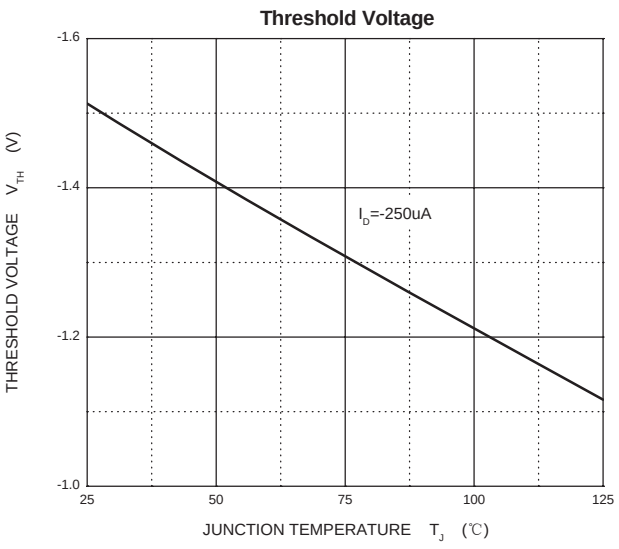






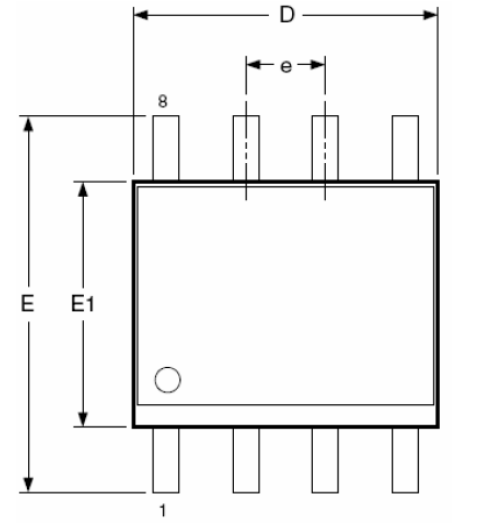


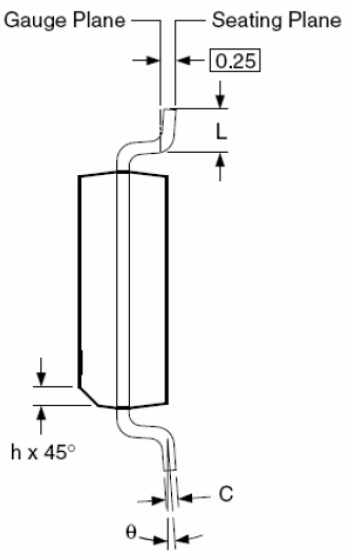


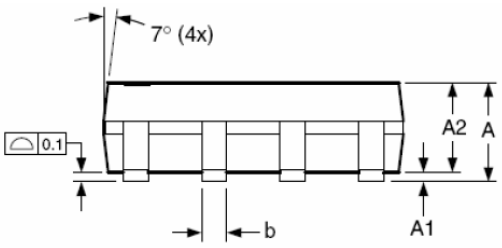


SOP-8 PACKAGE INFORMATION

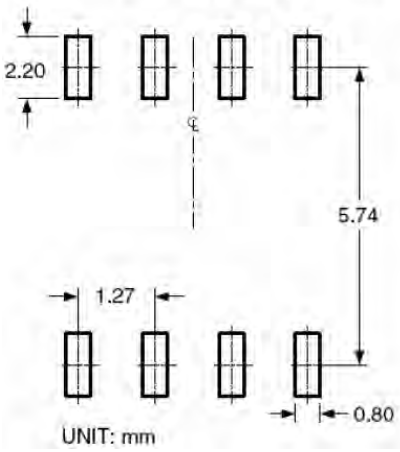
Dimensions in Millimeters (UNIT:mm)







RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
e	1.27 BSC		
E	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

Dimensions in inches

Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E1	0.150	0.154	0.157
e	0.050 BSC		
E	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

NOTES:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.