12V, 5.9mΩ, 15A, Dual N-Channel

V_{SSS}	$R_{SS(on)}$ Max	I_S Max
12 V	5.9 mΩ @ 4.5 V	15 A
	6.5 mΩ @ 3.8 V	
	8.2 mΩ @ 3.1 V	
	11.0 mΩ @ 2.5 V	

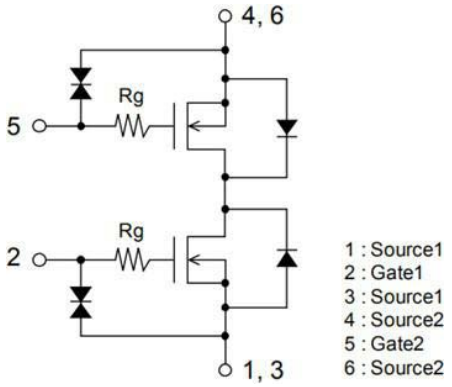
Features

- RSS(on) Max.= 5.9mΩ(VGS= 4.5V)
- 2 kV ESD HBM
- Common-Drain Type
- ESD protected gate
- Pb-Free, Halogen Free and RoHS compliance

CSDFN (Chip scale DFN)
2.11(mm)×1.18(mm)×0.50 (mm)

Applications

- Lithium ion battery



Schematic diagram

Absolute Maximum Ratings at Ta=25℃ (Note 1)

Parameter	Symbol	Maximum	Units
Source to Source Voltage	V_{SSS}	12	V
Gate to Source Voltage	V_{GSS}	8	V
Source Current (DC)	I_S	15	A
Source Current (Pulse) PW≤10μs, duty cycle≤1%	I_{SP}	60	A
Total Dissipation (Note 2)	P_T	1.5	W
Junction Temperature	T_j	150	℃
Storage Temperature	Tstg	55 to +150	℃

Note 1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Junction to Ambient (Note 2)	$R_{\theta JA}$	83	℃/W

Note 2 : Surface mounted on ceramic substrate (5000 mm^2 ×0.8 mm).

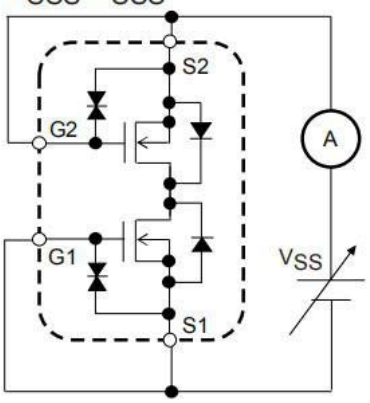
Electrical characteristics at T_a =25℃ (Note 3)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units
Source to Source Breakdown Voltage	$V_{(BR)SSS}$	IS = 1 mA, VGS = 0 V (Test Circuit 1)	12			V
Zero-Gate Voltage Source Current	I_{SSS}	VSS = 10 V, VGS = 0 V (Test Circuit 1)			1	μA
Gate to Source Leakage Current	I_{GSS}	VGS = ±8V, VSS = 0 V (Test Circuit 2)			±1	μA
Gate Threshold Voltage	$V_{GS(th)}$	VSS = 6 V, IS = 1 mA (Test Circuit 3)	0.4		1.3	V
Static Source to Source On-State Resistance	$R_{SS(on)}$	IS = 5 A, VGS = 4.5 V (Test Circuit 4)	3.1	4.5	5.9	mΩ
		IS = 5 A, VGS = 3.8 V (Test Circuit 4)	3.5	5.0	6.5	mΩ
		IS = 5 A, VGS = 3.1 V (Test Circuit 4)	4.0	5.8	8.2	mΩ
		IS = 5 A, VGS = 2.5 V (Test Circuit 4)	5.2	7.5	11.0	mΩ
Turn-ON Delay Time	$td_{(on)}$	VSS = 6 V, VGS = 4.5 V, IS = 3 A (Test Circuit 5)		180		ns
Rise Time	tr			300		ns
Turn-OFF Delay Time	$td_{(off)}$			1,700		ns
Fall Time	tf			660		ns
Total Gate Charge	Qg	VSS = 6 V, VGS = 4.5V, IS = 15 A (Test Circuit 6)		36		nC
Forward Source to Source Voltage	VF(S-S)	IS=3A, VGS=0 (Test Circuit 7)		0.76		V

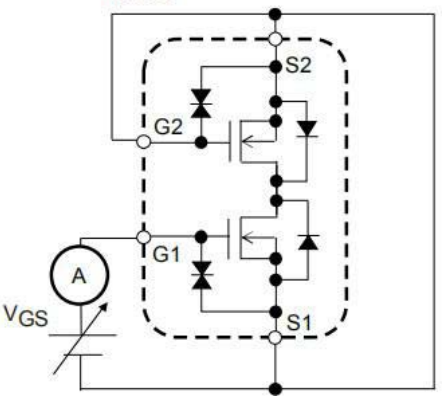
Note 3 : Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted.Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Measurement circuits

Test Circuit 1
V_{SSS} / I_{SSS}

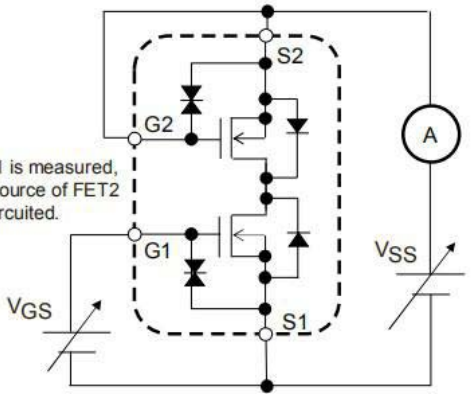


Test Circuit 2
I_{GSS}



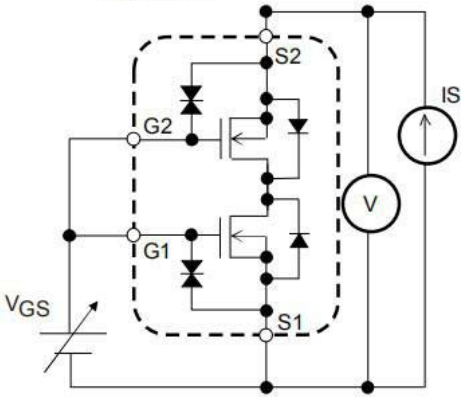
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
$V_{GS(th)}$

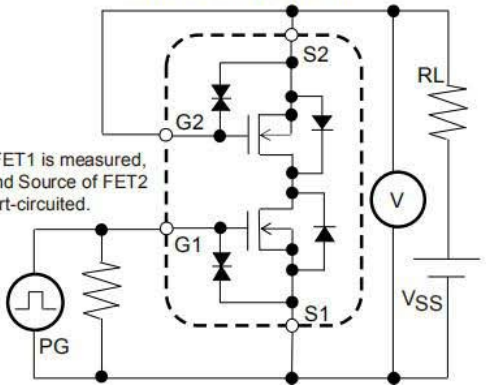


When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 4
$R_{SS(on)}$

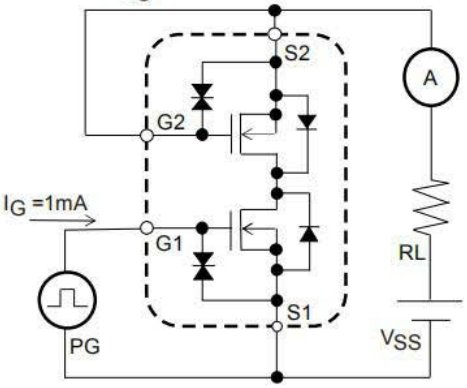


Test Circuit 5
$t_{d(on)}$, t_r, $t_{d(off)}$, t_f



When FET1 is measured, Gate and Source of FET2 are short-circuited.

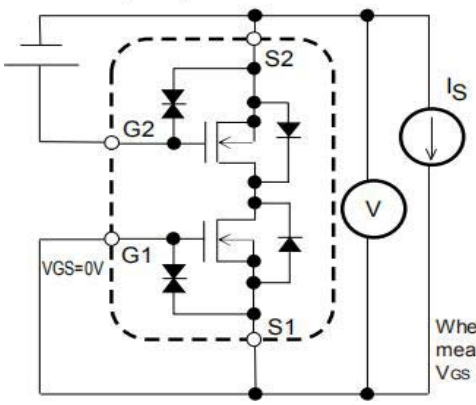
Test Circuit 6
Qg



When FET1 is measured, Gate and Source of FET2 are short-circuited.

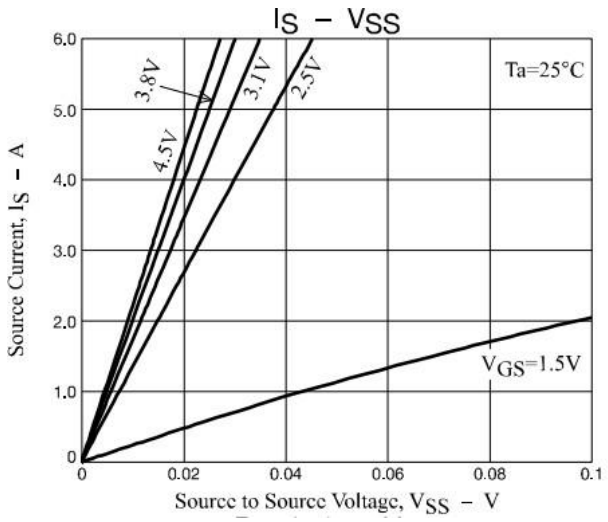
Measurement circuits(Con.)

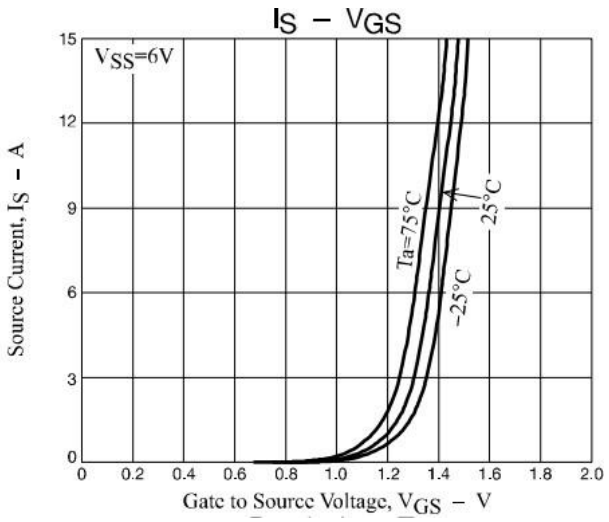
Test Circuit 7
$V_{F(S-S)}$

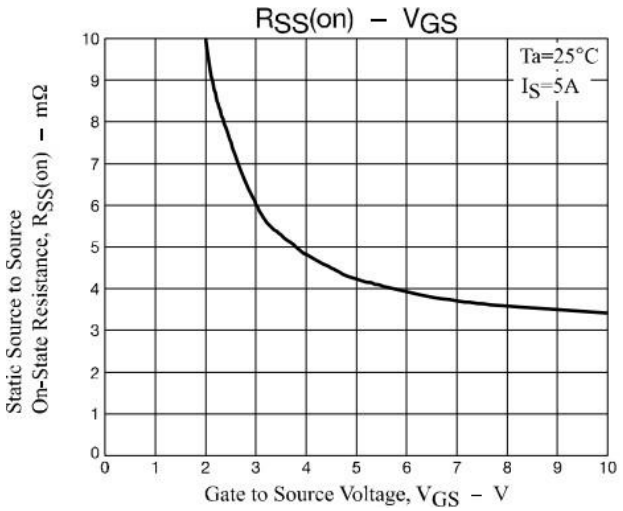


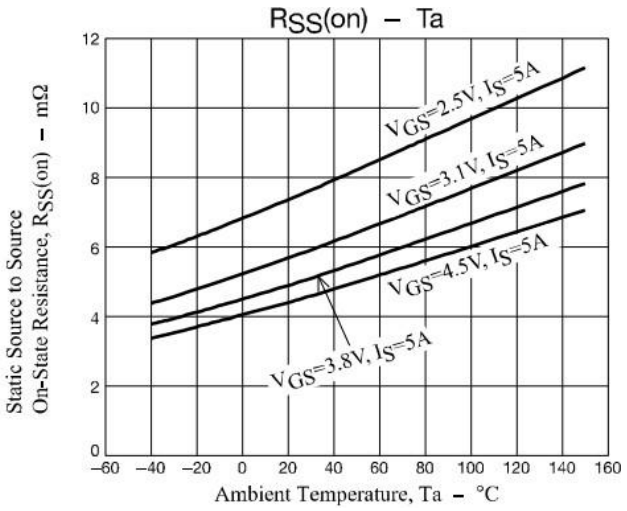
When FET1 is measured,+4.5V is added to V_{GS} of FET2.

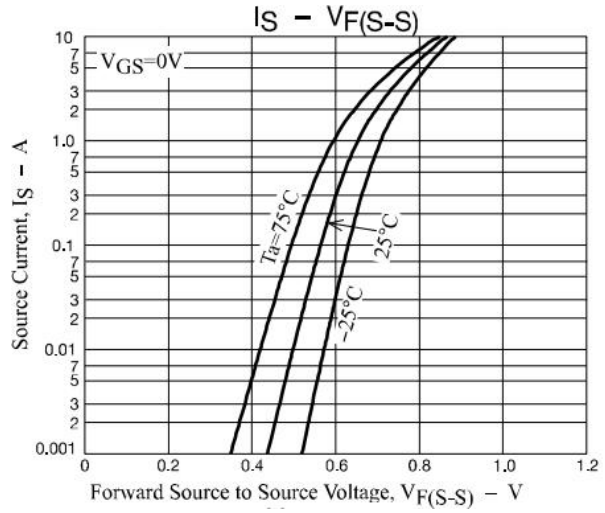
Electrical Characteristics Curves

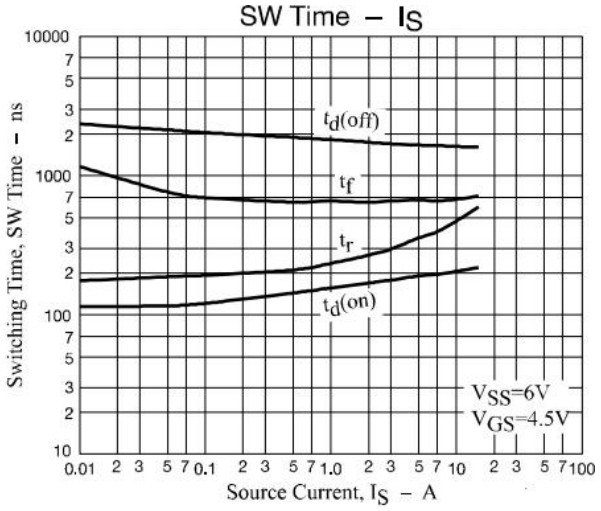




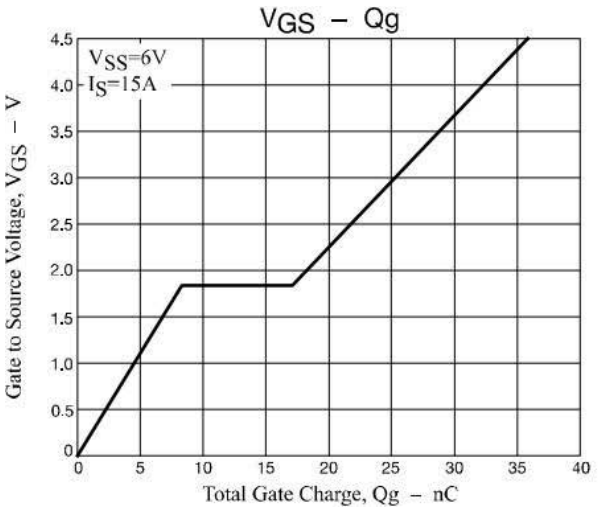


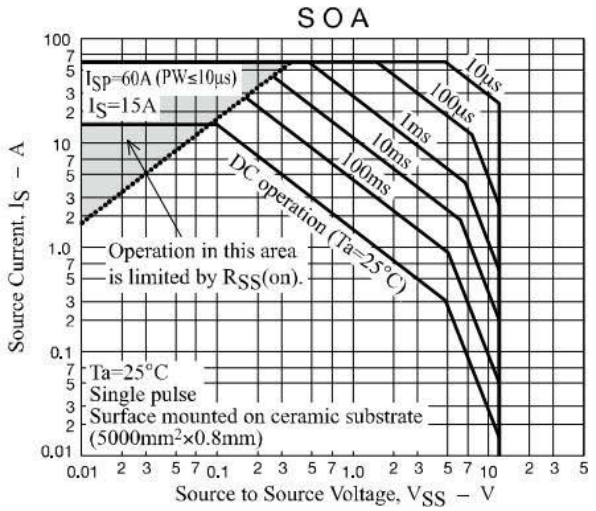


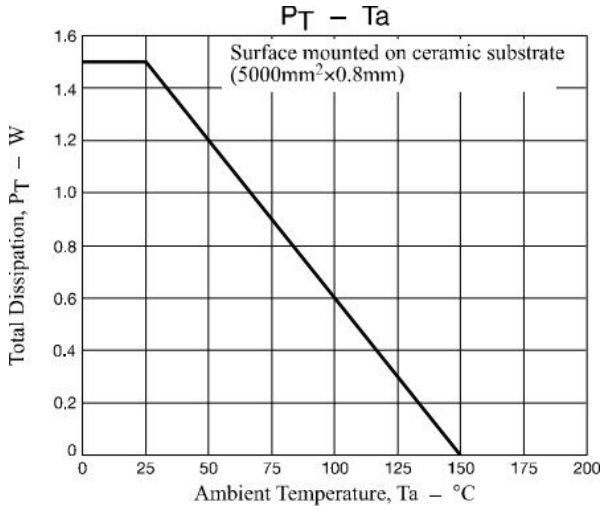


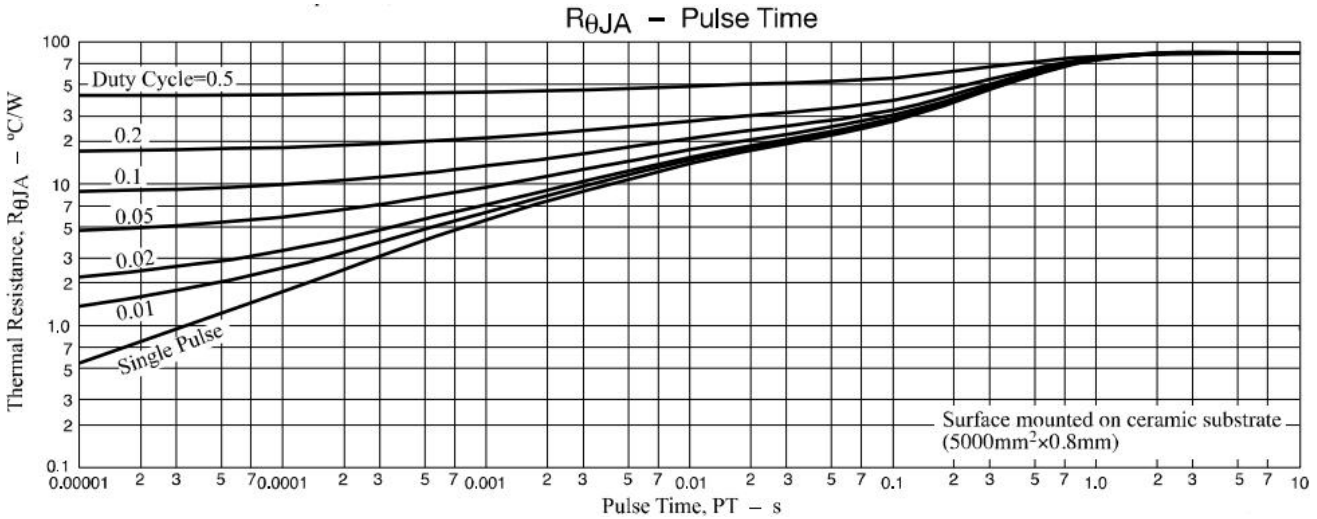


Electrical Characteristics Curves(Con.)

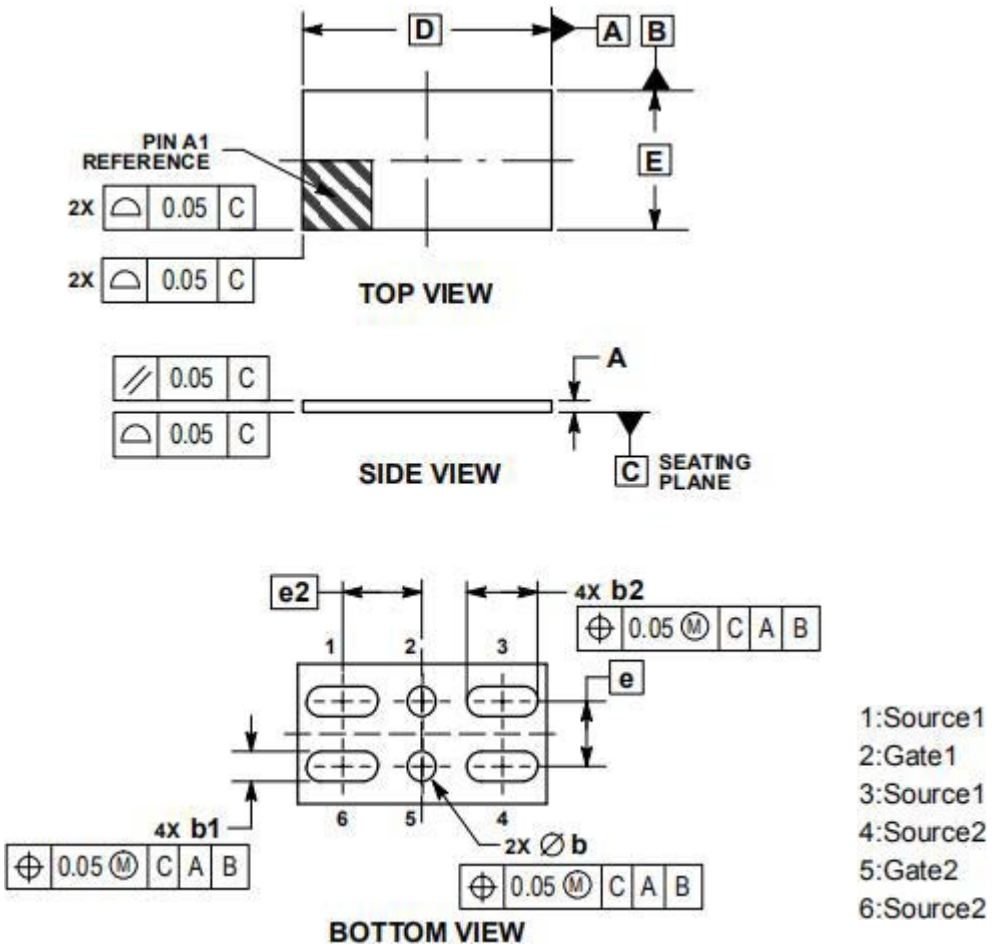








Package Dimensions(CSDFN)



Symbol	Millimeters（mm）		Symbol	Millimeters（mm）
	Min.	Max.		
A	0.47	0.53	D	2.11 BSC
b	0.22	0.28	E	1.18 BSC
b1	0.27	0.33	e	0.55 BSC
b2	0.575	0.635	e2	0.6775 BSC