N-Channel Enhancement Mode Field Effect Transistor

Product Summary

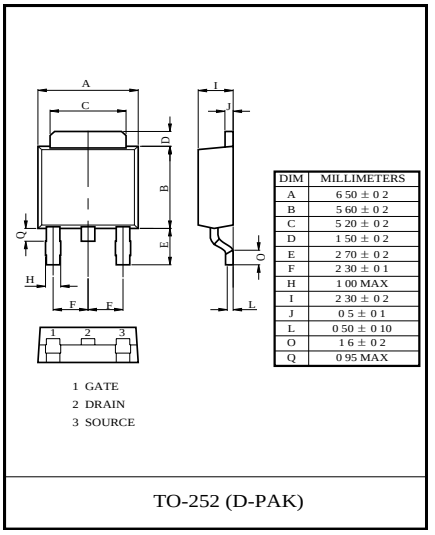
- V_{DS} 100V
- I_D 45A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜17 mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜21.5 mohm
- 100% UIS Tested
- 100% □VDS Tested

General Description

- Low $R_{DS(on)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Fast switching and soft recovery

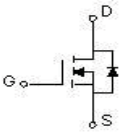
Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



DIM	MILLIMETERS
A	6.50 ± 0.2
B	5.60 ± 0.2
C	5.20 ± 0.2
D	1.50 ± 0.2
E	2.70 ± 0.2
F	2.30 ± 0.1
H	1.00 MAX
I	2.30 ± 0.2
J	0.5 ± 0.1
L	0.50 ± 0.10
O	1.6 ± 0.2
Q	0.95 MAX

TO-252 (D-PAK)



■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_C=25℃	I_D	45	A
	T_C=100℃		28.5	
Pulsed Drain Current [A]		I_{DM}	180	A
Avalanche energy [B]		EAS	81	mJ
Total Power Dissipation [C]	Tc=25℃	P_D	72	W
	Tc=100℃		28.8	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	t≤10S	$R_{\theta JA}$	15	20	℃/W
Thermal Resistance Junction-to-Ambient [D]	Steady-State		40	50	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.35	1.7	

■ Electrical Characteristics (T_j=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1	1.8	3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=20A		14	17	mΩ
		V_{GS}= 4.5V, I_D=20A		17	21.5	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V			1.3	V
Maximum Body-Diode Continuous Current	I_S				45	A
Gate resistance	R_G	f= 1 MHz, Open drain		1		Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHZ		1135		pF
Output Capacitance	C_{oss}			399		
Reverse Transfer Capacitance	C_{rss}			18		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=25A		16		nC
Gate-Source Charge	Q_{gs}			5.6		
Gate-Drain Charge	Q_{gd}			2.4		
Reverse Recovery Chrage	Q_{rr}	I_F=20A, di/dt=100A/us		42		
Reverse Recovery Time	t_{rr}			39.8		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=50V,I_D=25A R_{GEN}=2.2Ω		39.2		
Turn-on Rise Time	t_r			11		
Turn-off Delay Time	$t_{D(off)}$			53.2		
Turn-off fall Time	t_f			15.8		

A. Repetitive rating; pulse width limited by max. junction temperature.
B. V_{DD}=50V, V_{GS}=10V, L=5mH, I_{AS}=5.7A.
C. Pd is based on max. junction temperature, using junction-case thermal resistance.
D. The value of RqJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C. The Power dissipation PDSM is based on R qJA t≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

■ Typical Performance Characteristics

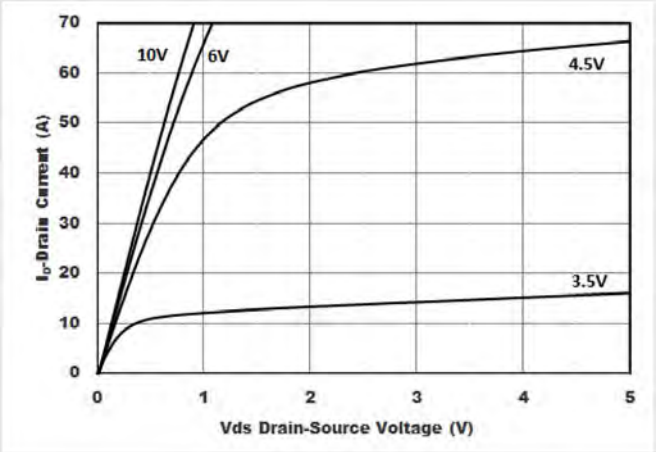


Figure1. Output Characteristics

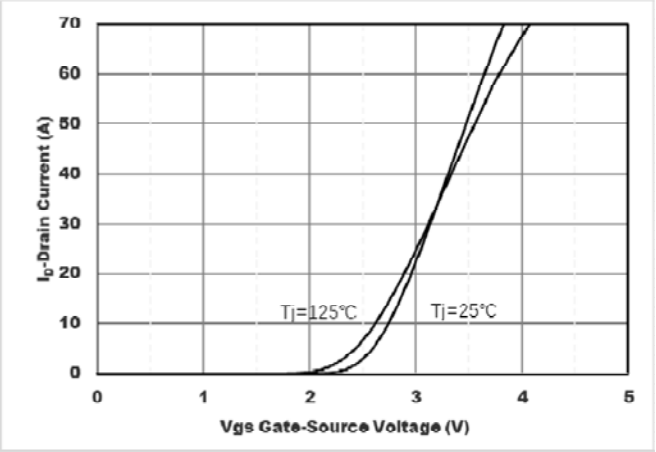


Figure2. Transfer Characteristics

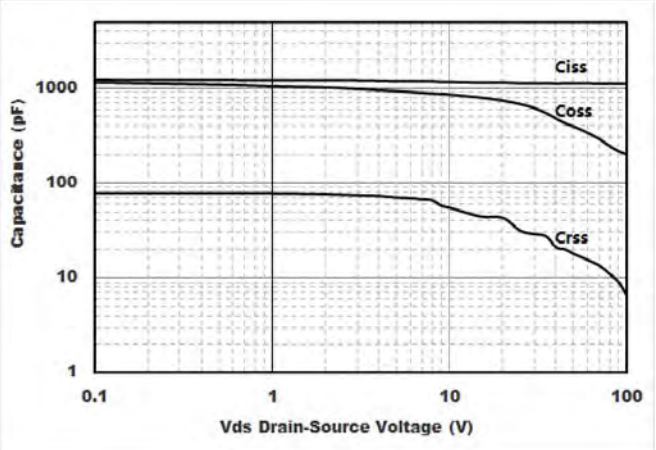


Figure3. Capacitance Characteristics

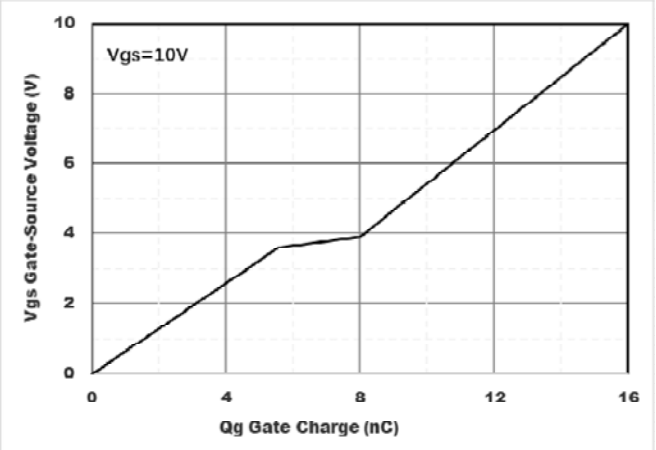


Figure4. Gate Charge

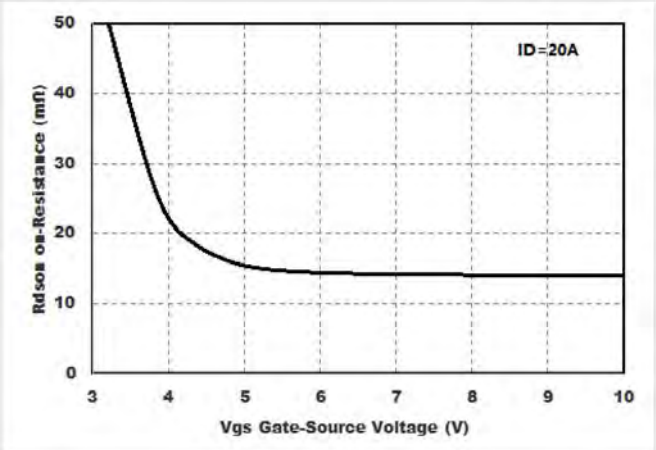


Figure5. : On-Resistance vs. Drain Current and Gate Voltage

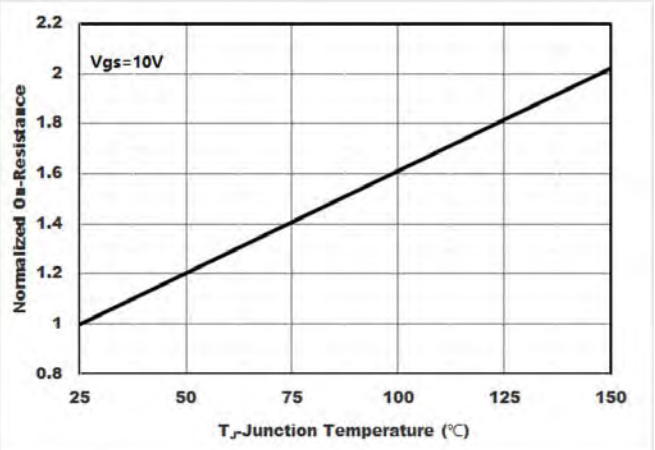


Figure6.Normalized On-Resistance

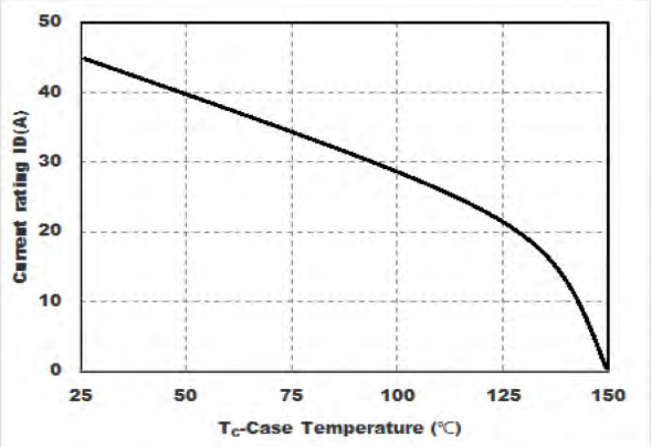


Figure7. Drain current

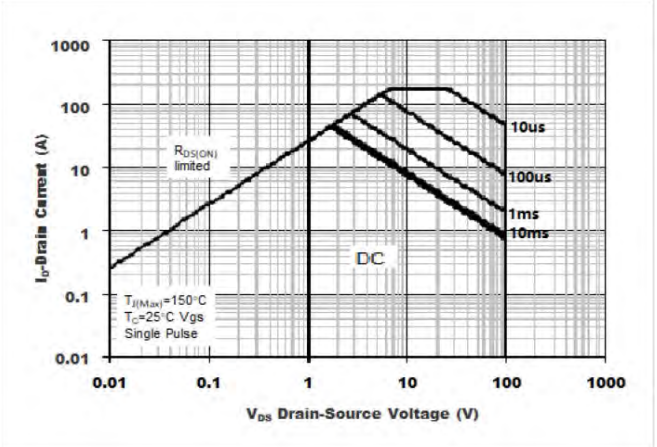


Figure8.Safe Operation Area

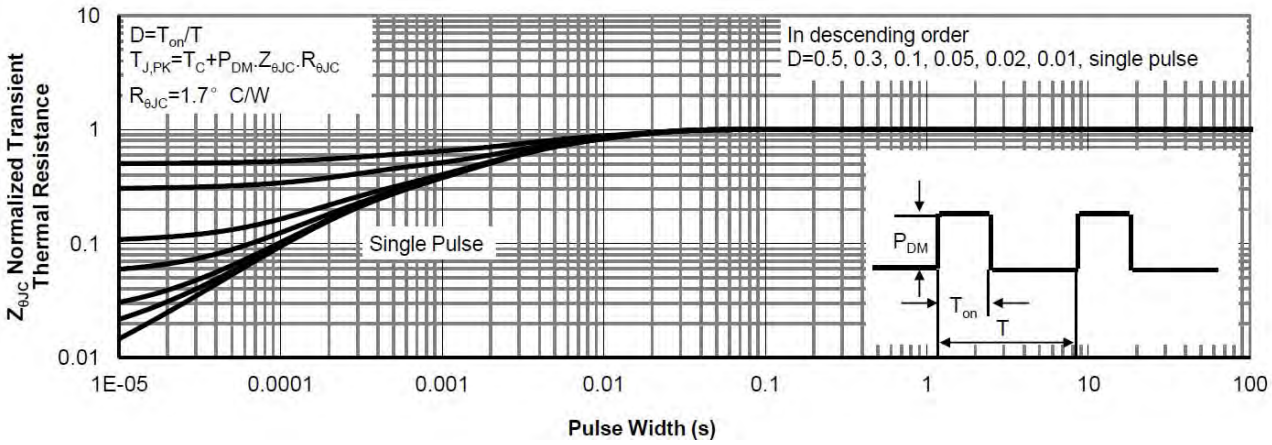


Figure9.Normalized Maximum Transient thermal impedance