

40V N-Channel MOSFETs

General Description

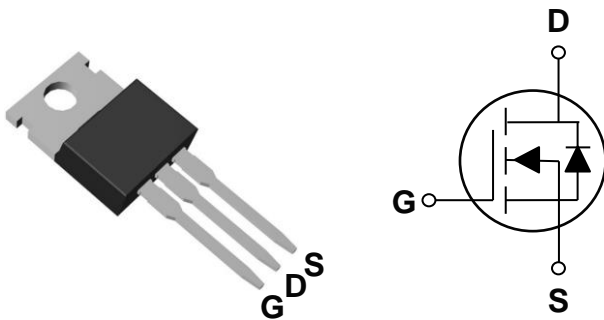
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

BVDSS	RDS(ON)	ID
40V	2.5mΩ	160A

Features

- 40V, 160A, $R_{DS(ON)} = 2.5m\Omega @ V_{GS} = 10V$
- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- Green Device Available

TO220 Pin Configuration



Applications

- MB / VGA / Server Vcore
- POL Applications
- SMPS 2nd SR
- BMS System

Absolute Maximum Ratings

$T_c=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous ($T_c=25^\circ\text{C}$) (Chip Limitation)	160	A
	Drain Current – Continuous ($T_c=100^\circ\text{C}$) (Chip Limitation)	100	A
I_{DM}	Drain Current – Pulsed ¹	640	A
EAS	Single Pulse Avalanche Energy ²	360	mJ
IAS	Single Pulse Avalanche Current ²	85	A
P_D	Power Dissipation ($T_c=25^\circ\text{C}$)	184	W
	Power Dissipation – Derate above 25°C	1.47	W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction to ambient	---	62	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance Junction to Case	---	0.68	$^\circ\text{C}/\text{W}$



FTK4902P

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Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Static State Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	40	---	---	V
I _{DSS}	Drain-Source Leakage Current	V _{DS} =40V, V _{GS} =0V, T _J =25 °C	---	---	1	uA
		V _{DS} =32V, V _{GS} =0V, T _J =85 °C	---	---	10	uA
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
R _{DS(ON)}	Static Drain-Source On-Resistance ³	V _{GS} =10V, I _D =30A	---	2.1	2.5	mΩ
		V _{GS} =4.5V, I _D =15A	---	2.6	3.5	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1	1.6	2.5	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =15A	---	45	---	S

Dynamic Characteristics

Q _g	Total Gate Charge ^{3, 4}	V _{DS} =20V, V _{GS} =4.5V, I _D =10A	---	70	140	nC
Q _{gs}	Gate-Source Charge ^{3, 4}		---	15	32	
Q _{gd}	Gate-Drain Charge ^{3, 4}		---	40	80	
T _{d(on)}	Turn-On Delay Time ^{3, 4}	V _{DD} =20V, V _{GS} =10V, R _G =10Ω I _D =10A	---	24.6	48	ns
T _r	Rise Time ^{3, 4}		---	62.8	120	
T _{d(off)}	Turn-Off Delay Time ^{3, 4}		---	224	440	
T _f	Fall Time ^{3, 4}		---	162	320	
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, F=1MHz	---	8000	12000	pF
C _{oss}	Output Capacitance		---	550	1000	
C _{rss}	Reverse Transfer Capacitance		---	420	800	
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz	---	1.2	2.4	Ω

Guaranteed Avalanche Energy

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy	V _{DD} =25V, L=0.1mH, I _{AS} =30A	45	---	---	mJ

Drain-Source Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current	V _G =V _D =0V, Force Current	---	---	160	A
I _{SM}	Pulsed Source Current ³		---	---	320	A
V _{SD}	Diode Forward Voltage ³	V _{GS} =0V, I _S =1A, T _J =25 °C	---	---	1	V
t _{rr}	Reverse Recovery Time	V _{GS} =0V, I _S =20A, di/dt=100A/μs	---	32	---	ns
Q _{rr}	Reverse Recovery Charge	T _J =25 °C	---	19	---	nC

Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=85A., R_G=25Ω, Starting T_J=25 °C.
3. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
4. Essentially independent of operating temperature.

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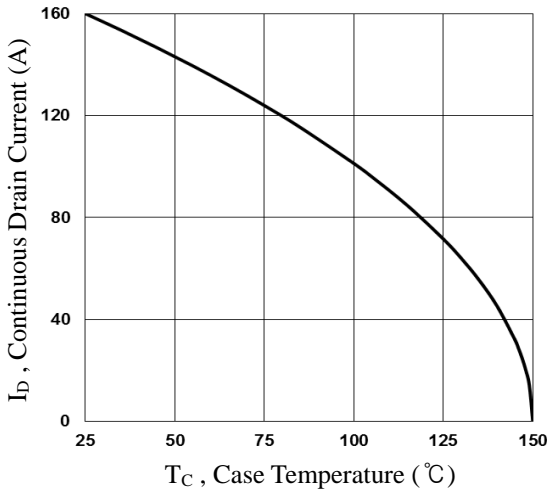


Fig.1 Conti nuous Drain Current vs. T_C

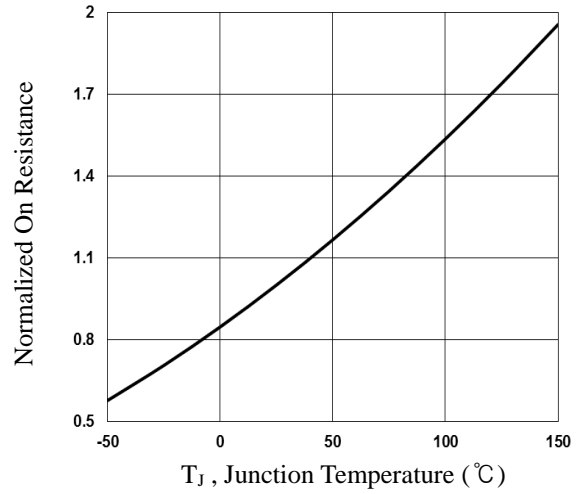


Fig.2 Normalized RDSON vs. T_J

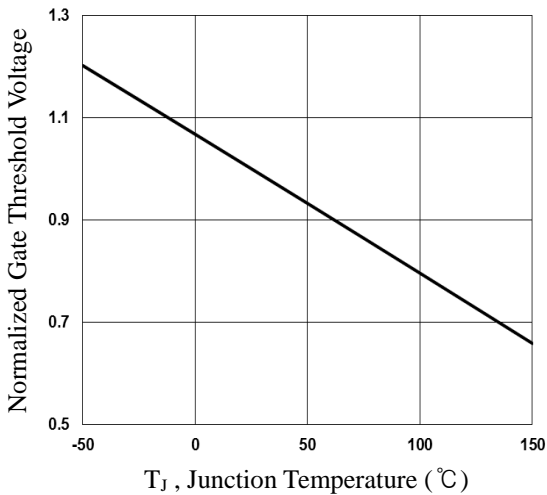


Fig.3 Normalized V_{th} vs. T_J

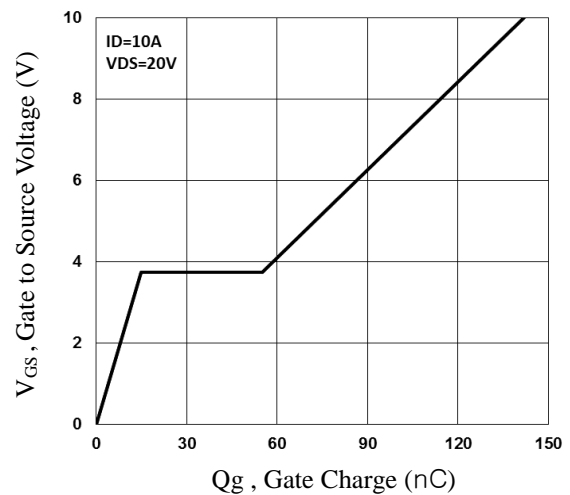


Fig.4 Gate Charge Waveform

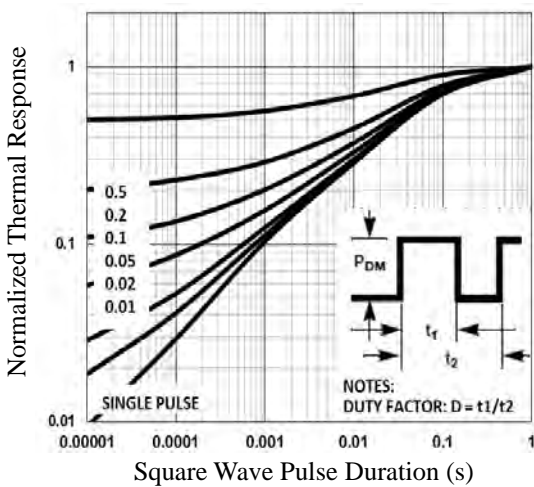


Fig.5 Normalized Transient Impedance

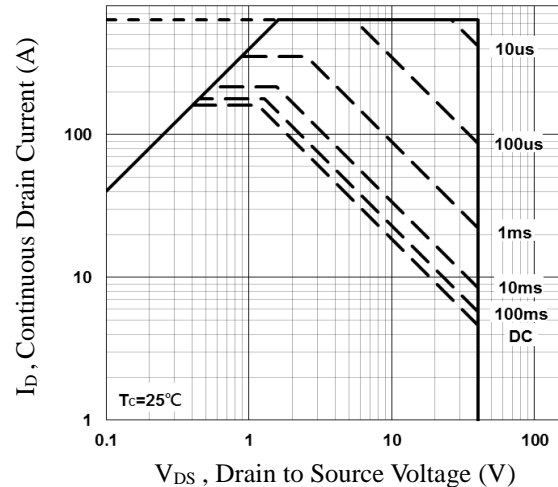


Fig.6 Maximum Safe Ope ration Area

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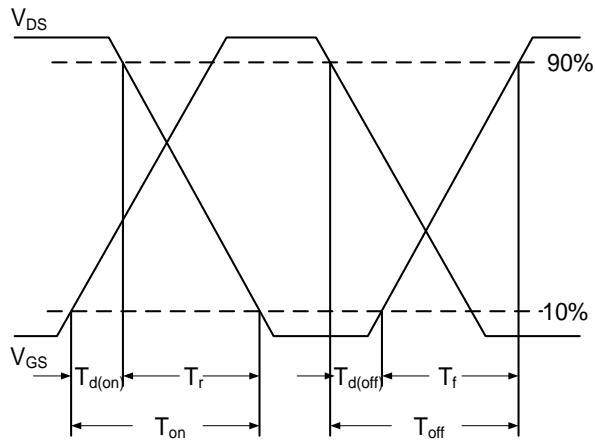


Fig. 7 Switching Time Waveform

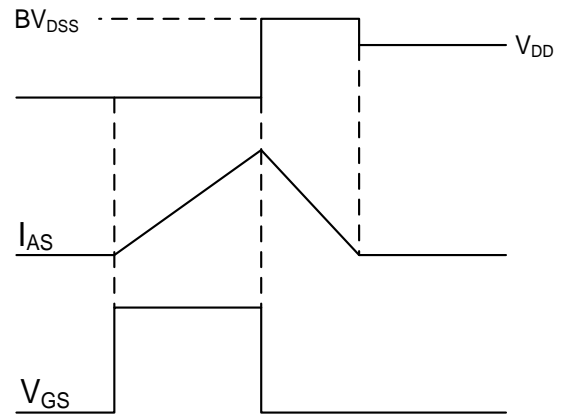
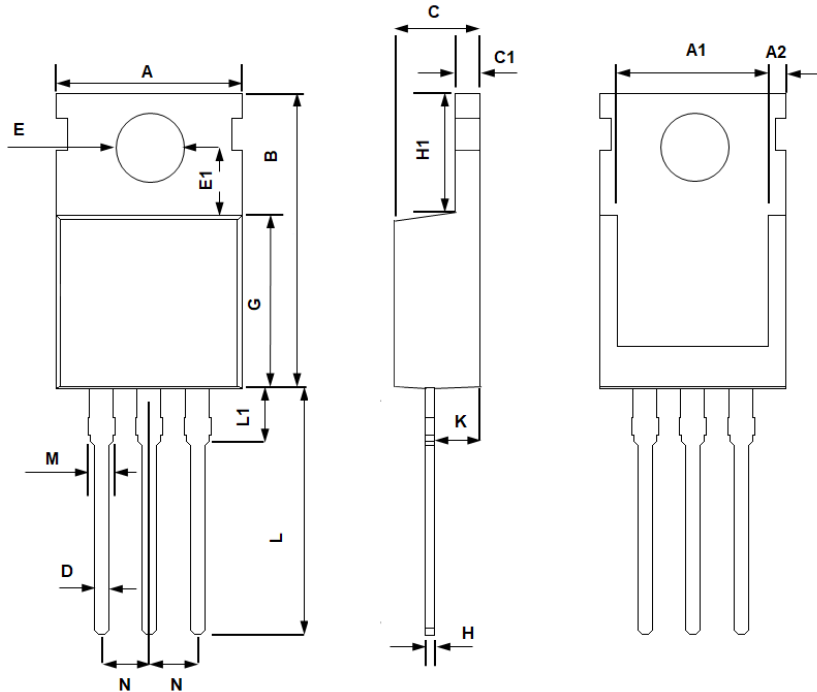


Fig. 8 EAS Waveform

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TO220 PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MAX	MIN	MAX	MIN
A	10.400	9.700	0.409	0.382
A1	8.900	7.400	0.350	0.291
A2	1.400	0.800	0.055	0.031
B	16.500	14.500	0.650	0.571
C	4.750	4.200	0.187	0.165
C1	1.500	1.100	0.059	0.043
D	1.000	0.600	0.039	0.024
E	4.000	3.300	0.157	0.130
E1	3.800	3.400	0.150	0.134
G	9.400	8.400	0.370	0.331
H	0.600	0.200	0.024	0.008
H1	6.850	6.200	0.270	0.244
K	2.850	2.100	0.112	0.083
L	14.000	12.500	0.551	0.492
L1	4.000	2.700	0.157	0.106
M	1.750	1.100	0.069	0.043
N	2.640	2.440	0.104	0.096