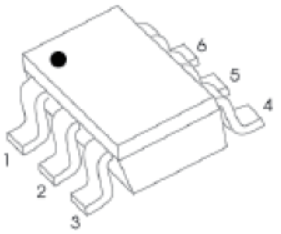
N channel+P Channel MOS FET

$V_{(BR)DSS}$	$R_{DS(on)}$MAX	I_D
20V	380mΩ@4.5V	0.75A
	450mΩ@2.5V	
	800mΩ@1.8V	
−20V	520mΩ@−4.5V	−0.66A
	700mΩ@−2.5V	
	950mΩ@−1.8V	

SOT- 363



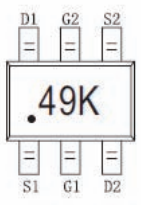
FEATURE

- Surface Mount Package
- Low R_{DS}(on)
- Operated at Low Logic Level Gate Drive
- ESD Protected Gate
- Including a N-ch FTK3134K and a P-ch FTK3139K (independently) In a Package

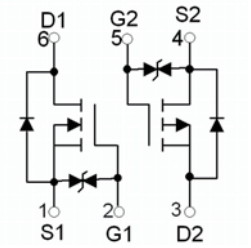
APPLICATION

- Load/ Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift

MARKING



Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
N- MOSFET			
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current (note 1)	I_D	0.75	A
Pulsed Drain Current (tp=10us)	I_{DM}	1.8	A
P- MOSFET			
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current (note 1)	I_D	-0.66	A
Pulsed Drain Current (tp=10us)	I_{DM}	-1.2	A
Temperature and Thermal Resistance			
Thermal Resistance from Junction to Ambient (note 1)	$R_{\theta JA}$	833	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~+150	℃
Lead Temperature for Soldering Purposes(1/8'' from case for 10 s)	T_L	260	℃

Electrical characteristics (T_a=25℃ unless otherwise noted)

N-ch MOSFET

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC CHAR ACTERISTICS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	20			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =20V,V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±12V, V_{DS} = 0V			±50	uA
Gate threshold voltage (note 2)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	0.35		1	V
Drain-source on-resistance(note 2)	$R_{DS(on)}$	V_{GS} =4.5V, I_D =0.65A			380	mΩ
		V_{GS} =2.5V, I_D =0.55A			450	mΩ
		V_{GS} =1.8V, I_D =0.45A			800	mΩ
Forward tranconductance(note 2)	g_{FS}	V_{DS} =10V, I_D =0.8A		1.6		S
Diode forward voltage	V_{SD}	I_S=0.15A, V_{GS} = 0V			1.2	V
DYNAMIC CHA RACTERISTICS (note 4)						
Input Capacitance	C_{iss}	V_{DS} =16V,V_{GS} =0V,f =1MHz		79	120	pF
Output Capacitance	C_{oss}			13	20	pF
Reverse Transfer Capacitance	C_{rss}			9	15	pF
SWITCHING CHARAC TERISTICS (note 3,4)						
Turn-on delay time	$t_{d(on)}$	V_{GS}=4.5V,V_{DS}=10V, I_D=500mA,R_{GEN}=10Ω		6.7		ns
Turn-on rise time	t_r			4.8		ns
Turn-off delay time	$t_{d(off)}$			17.3		ns
Turn-off fall time	t_f			7.4		ns

P-ch MOSFET

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC CHAR ACTERISTICS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-20			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-20V,V_{GS} = 0V			-1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±12V, V_{DS} = 0V			±20	uA
Gate threshold voltage (note 2)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-0.35		-1.1	V
Drain-source on-resistance(note 2)	$R_{DS(on)}$	V_{GS} =-4.5V, I_D =-1A			520	mΩ
		V_{GS} =-2.5V, I_D =-0.8A			700	mΩ
		V_{GS} =-1.8V, I_D =-0.5A			950	mΩ
Forward tranconductance(note 2)	g_{FS}	V_{DS} =-10V, I_D =-0.54A		1.2		S
Diode forward voltage	V_{SD}	I_S=-0.5A, V_{GS} = 0V			-1.2	V
DYNAMIC CHA RACTERISTICS (note 4)						
Input Capacitance	C_{iss}	V_{DS} =-16V,V_{GS} =0V,f =1MHz		113	170	pF
Output Capacitance	C_{oss}			15	25	pF
Reverse Transfer Capacitance	C_{rss}			9	15	pF
SWITCHING CHARAC TERISTICS (note 3, 4)						
Turn-on delay time	$t_{d(on)}$	V_{GS}=-4.5V,V_{DS}=-10V, I_D=-200mA,R_{GEN}=10Ω		9		ns
Turn-on rise time	t_r			5.8		ns
Turn-off delay time	$t_{d(off)}$			32.7		ns
Turn-off fall time	t_f			20.3		ns

Notes :

1.Surface mounted on FR4 board using the minimum recommended pad size.

2. Pulse Test : Pulse width=300μs, duty cycle≤2%.

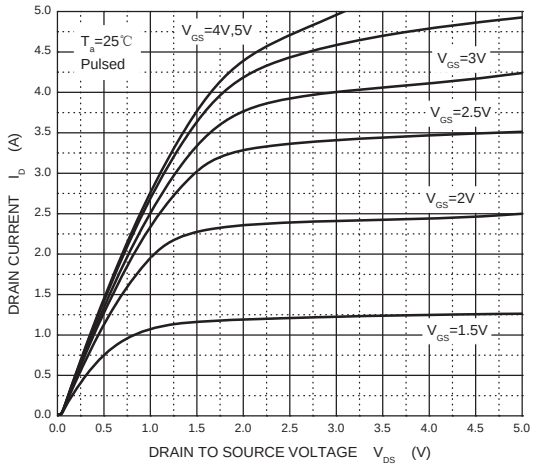
3. Switching characteristics are independent of operating junction temperature.

4. Graranted by design，not subject to producting.

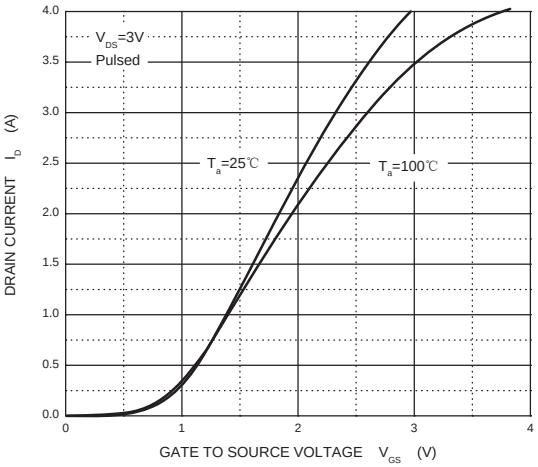
Typical Characteristics

N-Channel MOS

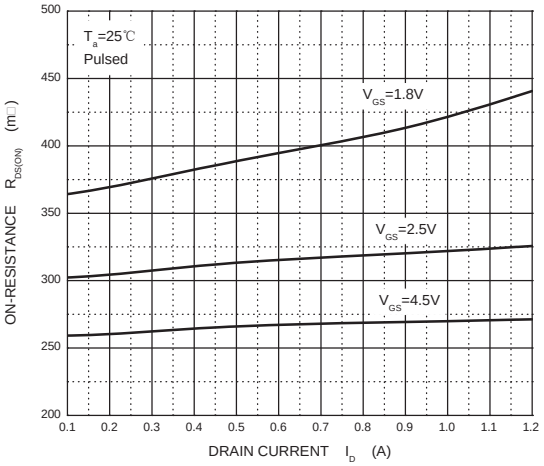
Output Characteristics



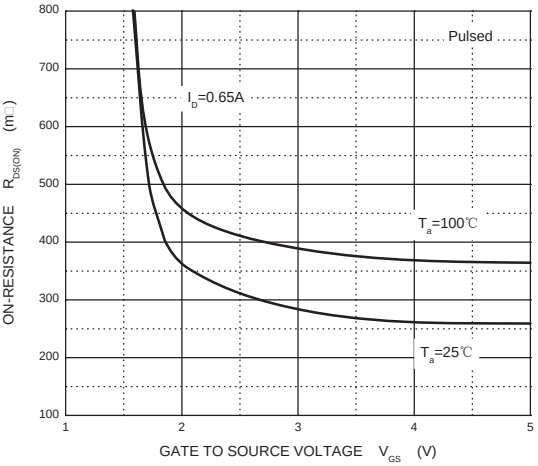
Transfer Characteristics



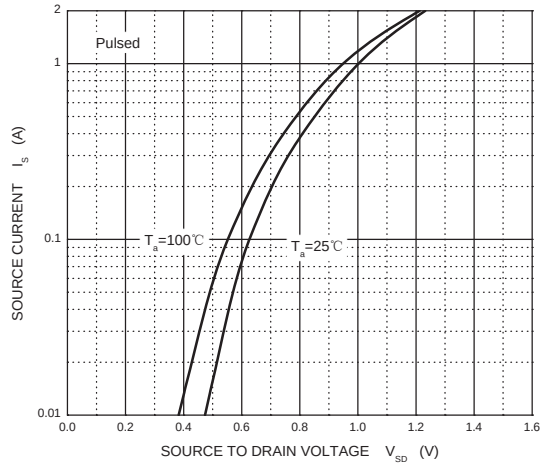
$R_{DS(ON)}$ —— I_D



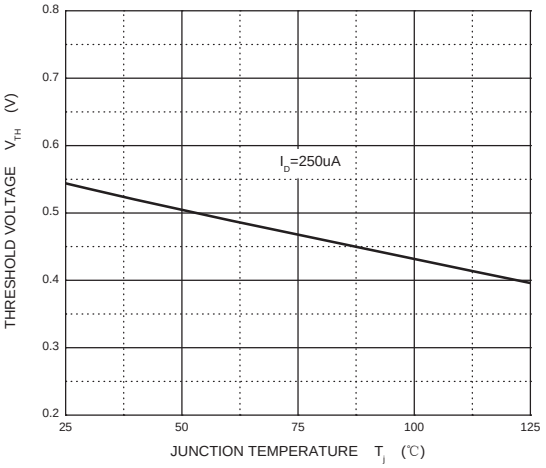
$R_{DS(ON)}$ —— V_{GS}



I_S —— V_{SD}

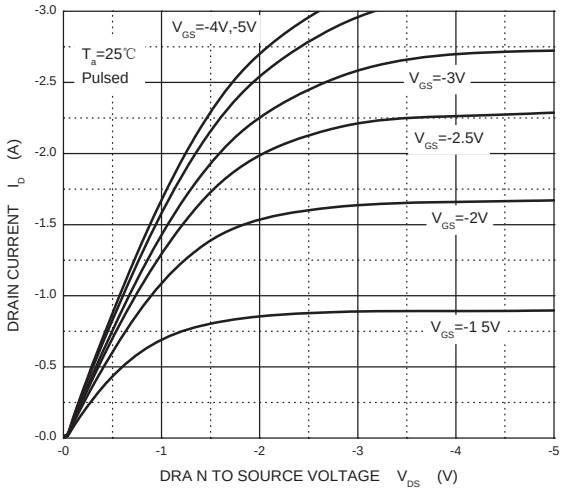


Threshold Vol tage

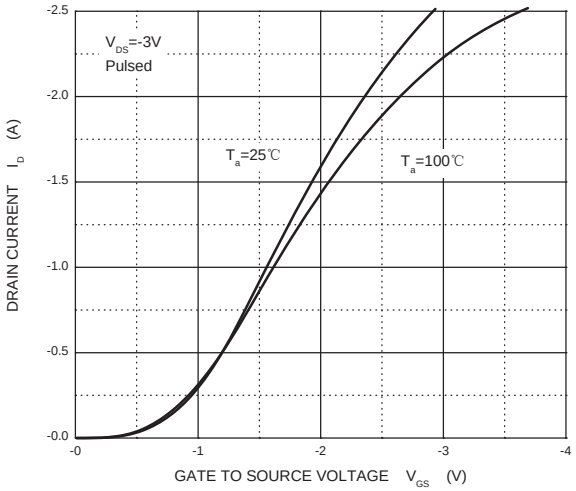


P-Channel MOS

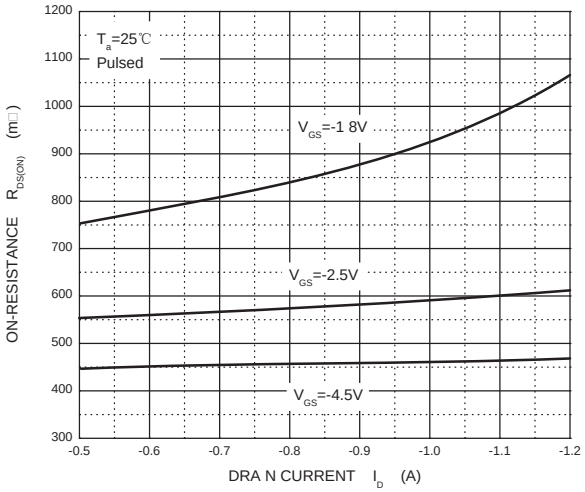
Output Characteristics



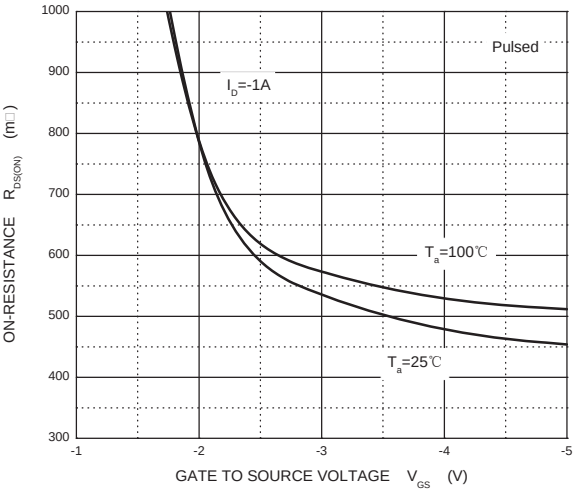
Transfer Characteristics



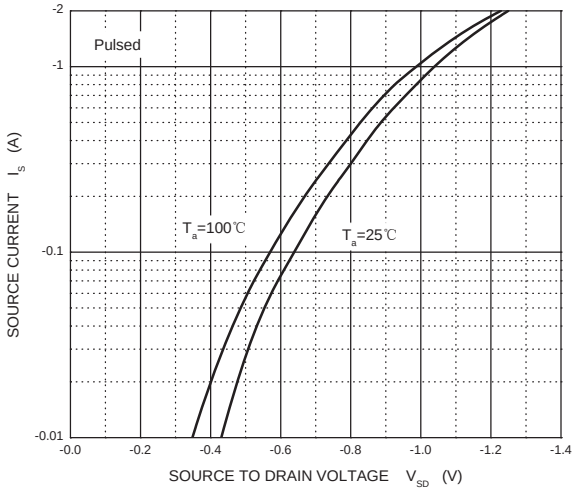
$R_{DS(ON)}$ —— I_D



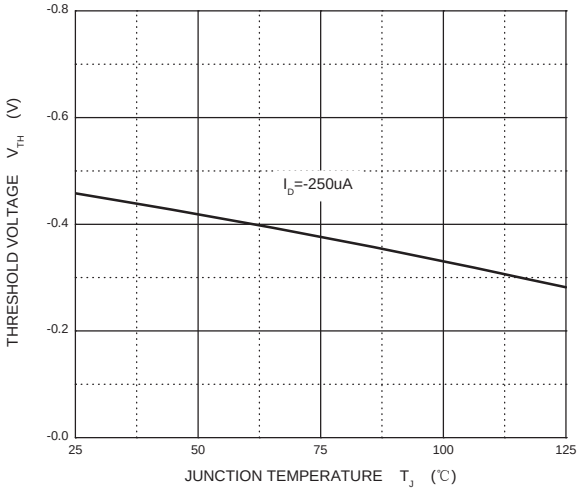
$R_{DS(ON)}$ —— V_{GS}



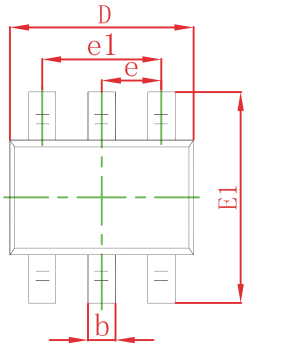
I_S —— V_{SD}

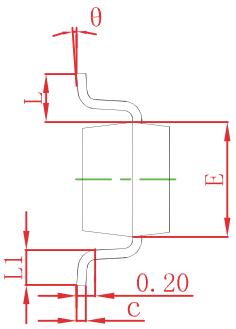


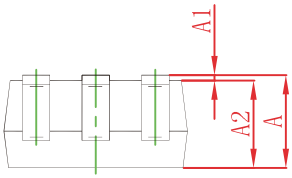
Threshold Volt age



SOT-363 Package Outline Dimensions

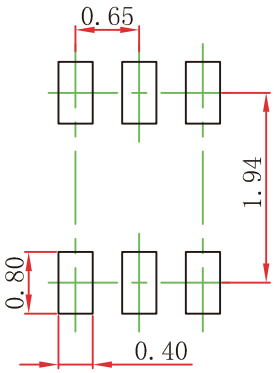






Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0 043
A1	0.000	0.100	0.000	0 004
A2	0.900	1.000	0.035	0 039
b	0.150	0.350	0.006	0 014
c	0.080	0.150	0.003	0 006
D	2.000	2.200	0.079	0 087
E	1.150	1.350	0.045	0 053
E1	2.150	2.450	0.085	0 096
e	0.650 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0 055
L	0.525 REF		0 021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

SOT-363 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.