

## N-Ch 100V Fast Switching MOSFETs

- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

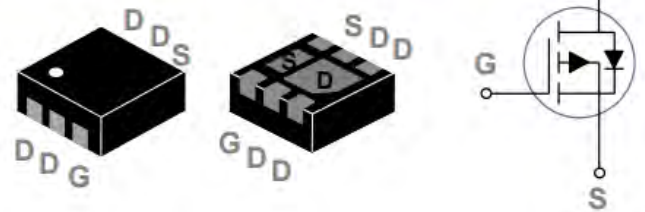
### Product Summary

BVDSS	RDSON	ID
100V	24mΩ	8A

### Description

The FTK2392DFN22 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The FTK2392DFN22 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

### DFN2x2-6L 2EP Pin Configuration



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	100	V
V <sub>GS</sub>	Gate-Source Voltage	± 20	V
I <sub>D</sub> @T <sub>A</sub> =25 °C	Continuous Drain Current <sup>1</sup>	8	A
I <sub>D</sub> @T <sub>A</sub> =70 °C	Continuous Drain Current <sup>1</sup>	6.4	A
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	32	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	29	mJ
I <sub>AS</sub>	Avalanche Current	24	A
P <sub>D</sub> @T <sub>A</sub> =25 °C	Total Power Dissipation <sup>4</sup>	2.7	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C

### Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R <sub>θJA</sub>	Thermal Resistance Junction-ambient <sup>1</sup> (t ≤ 10S)	---	45	°C/W
	Thermal Resistance Junction-ambient <sup>1</sup> (Steady State)	---	80	°C/W



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### Electrical Characteristics ( $T_J=25\text{ }^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=8A$	---	20	24	$m\Omega$
		$V_{GS}=4.5V, I_D=4A$	---	23	28	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	---	2.5	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V, T_J=25\text{ }^\circ\text{C}$	---	---	1	$\mu A$
		$V_{DS}=80V, V_{GS}=0V, T_J=85\text{ }^\circ\text{C}$	---	---	10	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$Q_g$	Total Gate Charge (10V)	$V_{DS}=30V, V_{GS}=10V, I_D=8A$	---	57	---	nC
$Q_{gs}$	Gate-Source Charge		---	8.7	---	
$Q_{gd}$	Gate-Drain Charge		---	14	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V, V_{GS}=10V, R_G=3.3\Omega, I_D=1A$	---	16.2	---	ns
$T_r$	Rise Time		---	41.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	56.4	---	
$T_f$	Fall Time		---	16.2	---	
$C_{iss}$	Input Capacitance	$V_{DS}=25V, V_{GS}=0V, f=1MHz$	---	3307	---	pF
$C_{oss}$	Output Capacitance		---	201	---	
$C_{rss}$	Reverse Transfer Capacitance		---	151	---	

### Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V$ , Force Current	---	---	8	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25\text{ }^\circ\text{C}$	---	---	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=8A, di/dt=100A/\mu s$ ,	---	44	---	nS
$Q_{rr}$	Reverse Recovery Charge	$T_J=25\text{ }^\circ\text{C}$	---	25	---	

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=24A$
- 4.The power dissipation is limited by  $150\text{ }^\circ\text{C}$  junction temperature
- 5.The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

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## Typical Characteristics

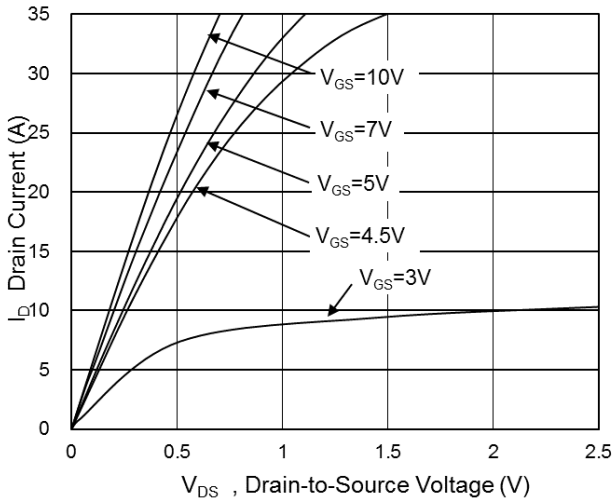


Fig.1 Typical Output Characteristics

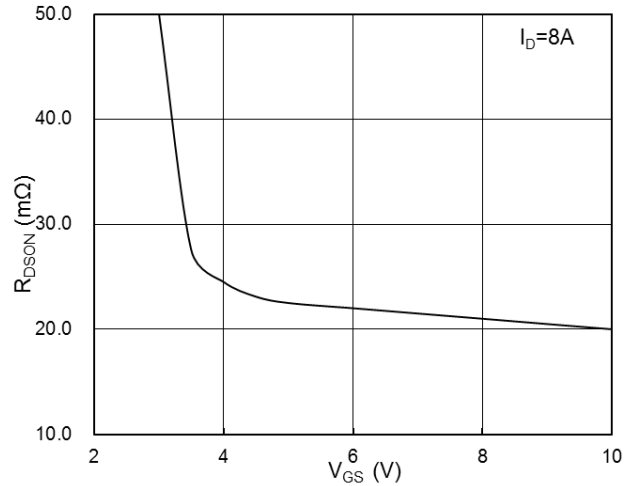


Fig.2 On-Resistance vs. G-S Voltage

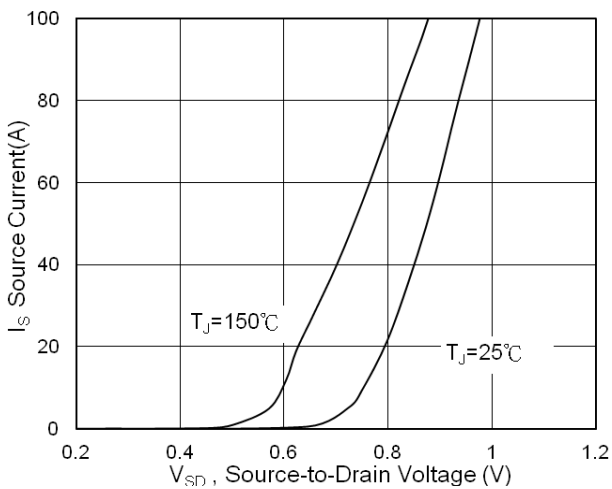


Fig.3 Source-Drain Diode Forward Voltage

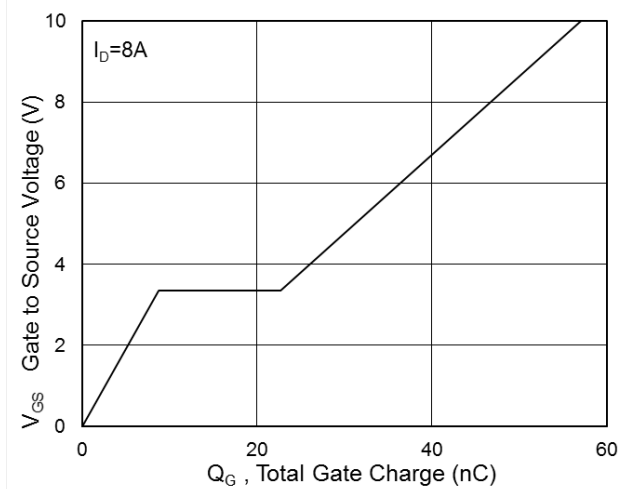


Fig.4 Gate-Charge Characteristics

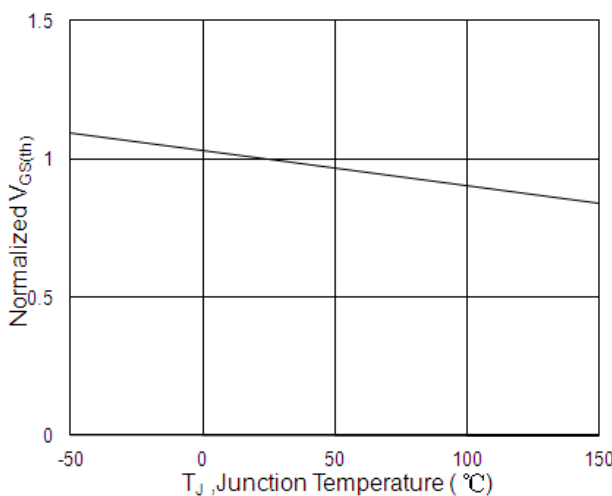


Fig.5 Normalized V<sub>GS(th)</sub> vs. T<sub>J</sub>

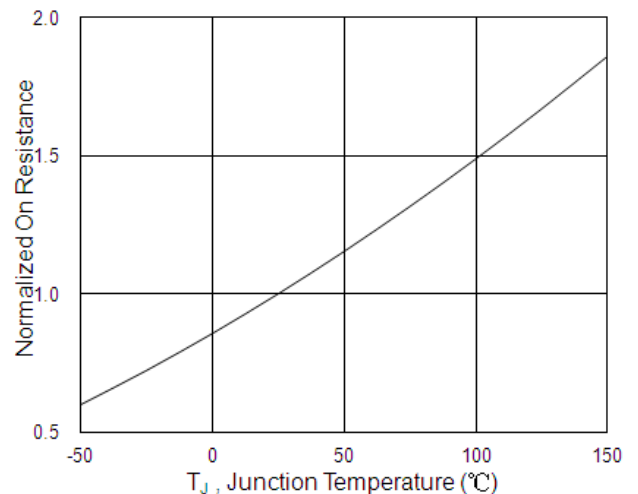
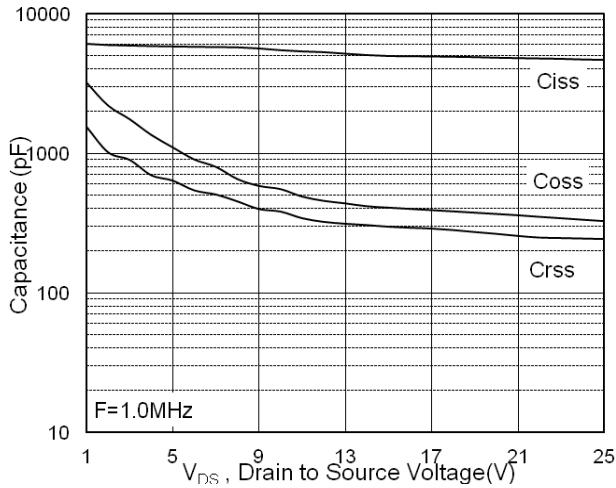
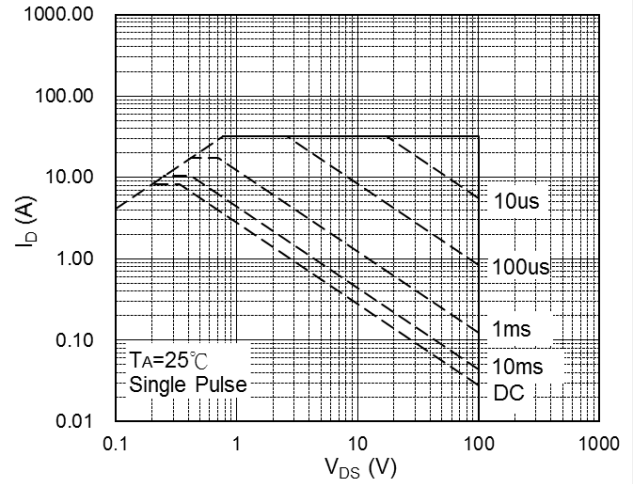


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>

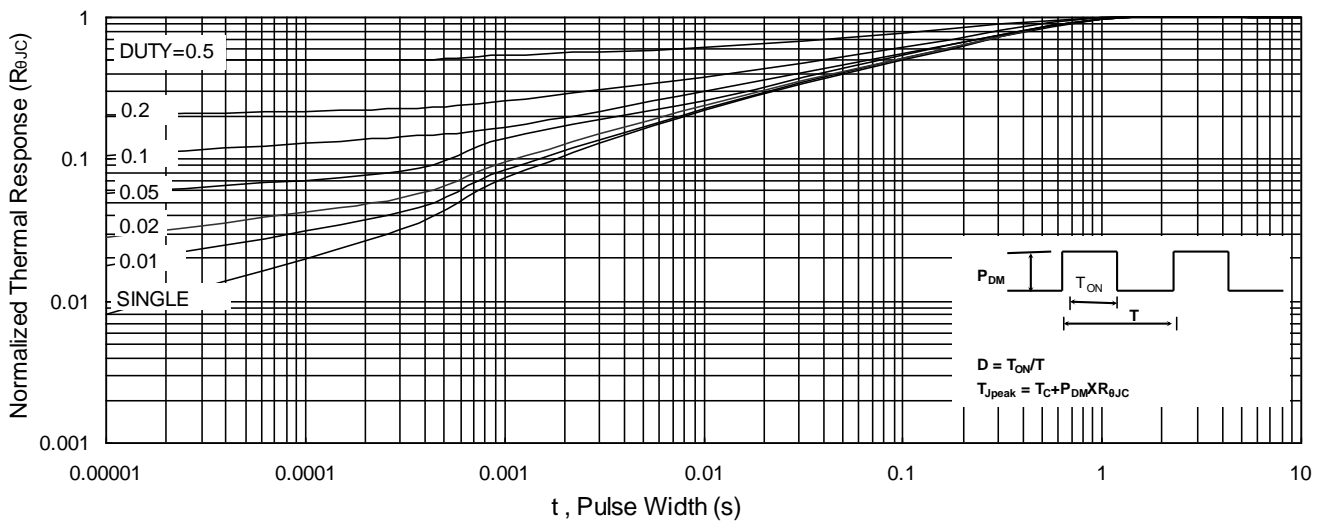
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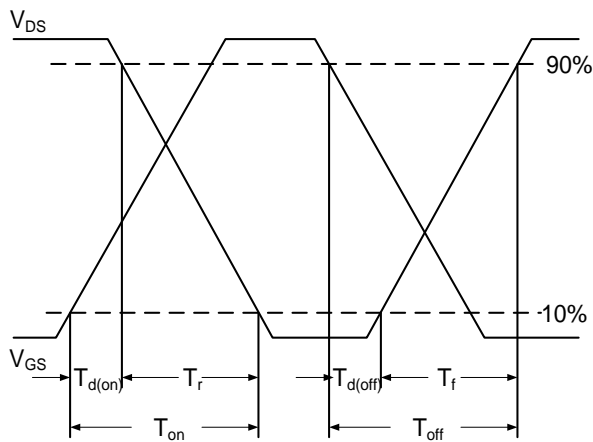
**Fig.7 Capacitance**



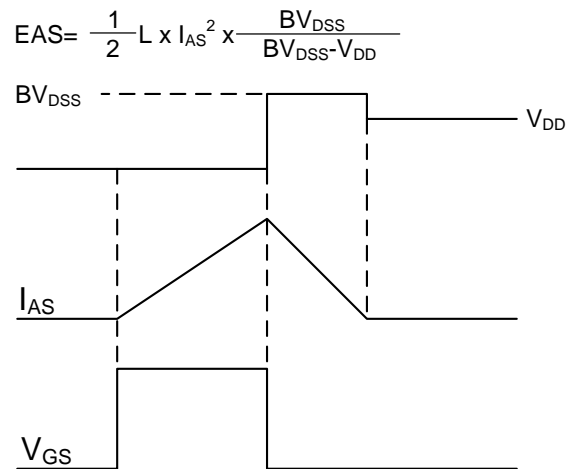
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**