

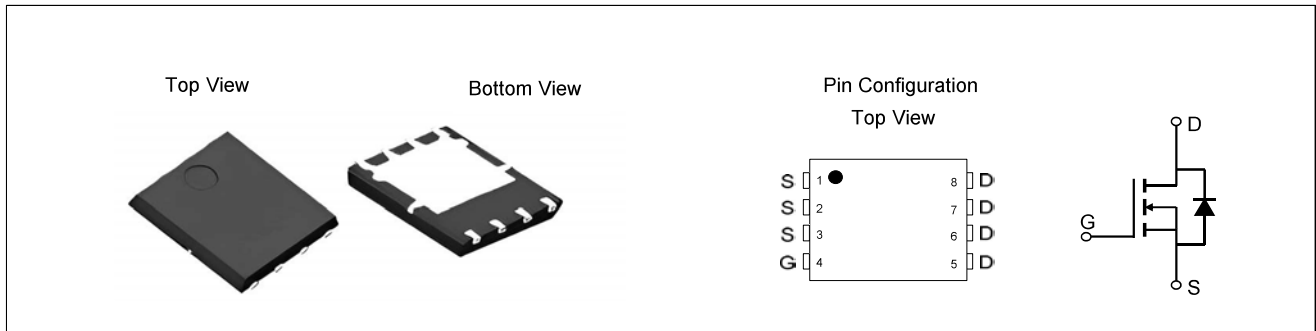
Feature

- ✧ Low $R_{DS(ON)}$
- ✧ Low Gate Charge
- ✧ High current Capability
- ✧ Green product RoHS compliant, lead free
- ✧ AEC-Q101 qualified

Product Summary

V_{DS}	40	V
$V_{GS(th_Typ)}$	3	V
$R_{DS(ON)_Typ}$ (@ $V_{GS} = 10V$)	1.1	m Ω
I_D (at $V_{GS} = 10V$) ⁽¹⁾	209	A

Type	Package	Marking	Outline	Media	Quantity (pcs)
FM16AGS04KVB	PDFN5x6-8L	M16AGS04VB	Tape	13" Reel	5000



Absolute Maximum Ratings (Rating at $T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ⁽¹⁾	I_D	$T_c=25^\circ C$	209
		$T_c=100^\circ C$	148
Pulsed Drain Current ⁽²⁾	I_{DM}	837	A
Body-Diode Continuous Current	I_S	209	A
Avalanche Current ⁽³⁾	I_{AS}	20	A
Avalanche Energy ⁽³⁾	E_{AS}	1314	mJ
Power Dissipation ⁽⁴⁾	P_D	$T_c=25^\circ C$	125
		$T_c=100^\circ C$	63
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +175	$^\circ C$



FM16AGS04KVB

Electrical Characteristics (Rating at $T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=40\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$	-	-	1 5	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2	3	4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=30\text{A}$	-	1.1	1.6	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=30\text{A}$	-	63	-	S
V_{SD}	Diode Forward Voltage	$I_S=30\text{A}$, $V_{GS}=0\text{V}$	-	0.78	1.2	V
DYNAMIC PARAMETERS ⁽⁵⁾						
C_{iss}	Input Capacitance		-	5540	11000	pF
C_{oss}	Output Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=20\text{V}$, $f=1\text{MHz}$	-	1968	4000	pF
C_{riss}	Reverse Transfer Capacitance		-	14.7	45	pF
R_g	Gate Resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	-	18.5	-	Ω
SWITCHING PARAMETERS ⁽⁵⁾						
Q_g	Total Gate Charge		-	70	110	nC
Q_{gs}	Gate Source Charge	$V_{GS}=0\sim 10\text{V}$, $V_{DS}=20\text{V}$, $I_D=50\text{A}$	-	28.5	45	nC
Q_{gd}	Gate Drain Charge		-	12.8	20	nC
$t_{D(on)}$	Turn-On Delay Time		-	12.8	25	ns
t_r	Turn-On Rise Time	$V_{GS}=10\text{V}$, $V_{DD}=20\text{V}$, $R_L=0.4\Omega$, $R_g=2.5\Omega$	-	48	100	ns
$t_{D(off)}$	Turn-Off Delay Time		-	62	120	ns
t_f	Turn-Off Fall Time		-	42	85	ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=50\text{A}$, $di/dt=100\text{A}/\mu\text{s}$	-	71.5	150	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=50\text{A}$, $di/dt=100\text{A}/\mu\text{s}$	-	146	300	nC

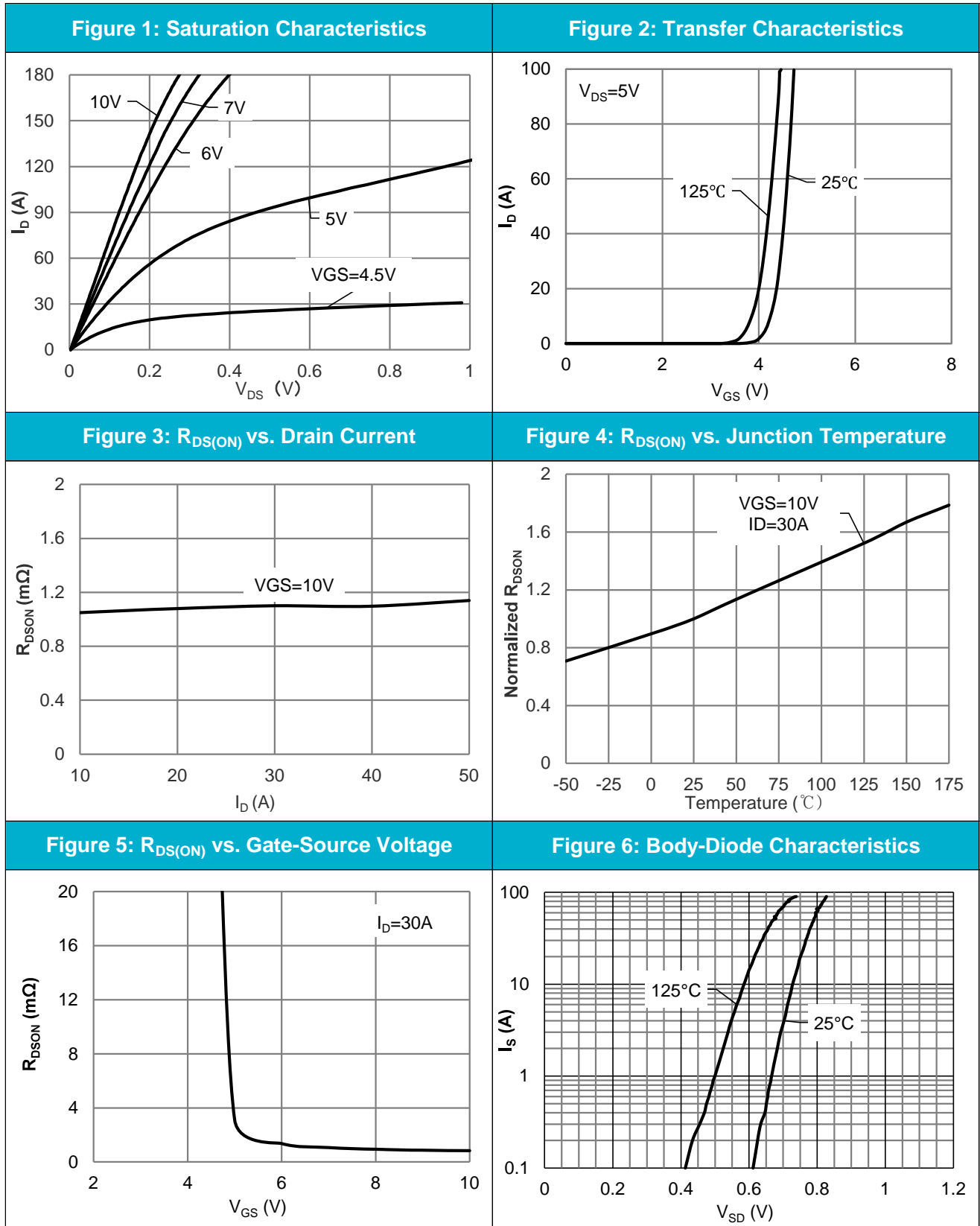
Thermal Resistances

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal resistance from junction to ambient	-	1.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal resistance from junction to ambient	-	45	$^\circ\text{C}/\text{W}$

Notes:

1. Computed continuous current assumes the condition of T_{J_Max} while the actual continuous depends on the thermal & electro-mechanical application board design.
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
3. This single-pulse measurement was taken under the following condition [$L=10\text{mH}$, $V_{GS}=10\text{V}$, $V_{DS}=30\text{V}$] while its value is limited by $T_{J_Max}=175^\circ\text{C}$.
4. The power dissipation P_D is based on $T_{J_Max}=175^\circ\text{C}$.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Electrical and Thermal Characteristics



Typical Electrical and Thermal Characteristics

Figure 7: Gate-Charge characteristics

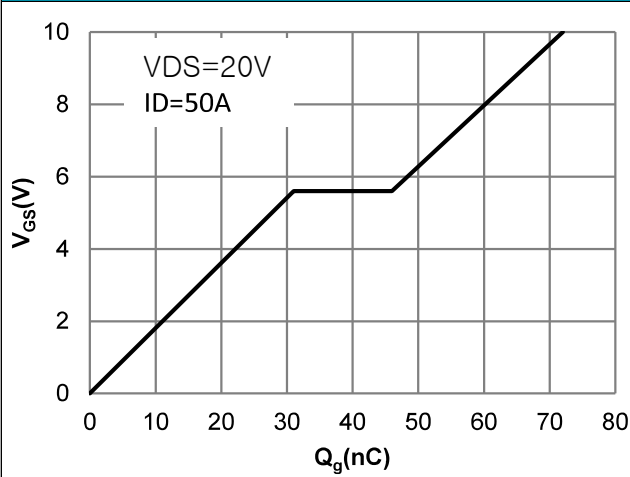


Figure 8: Capacitance characteristics

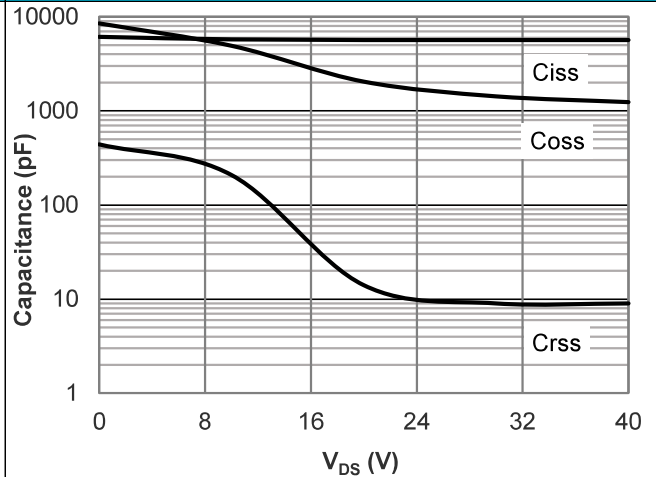


Figure 9: Current De-rating

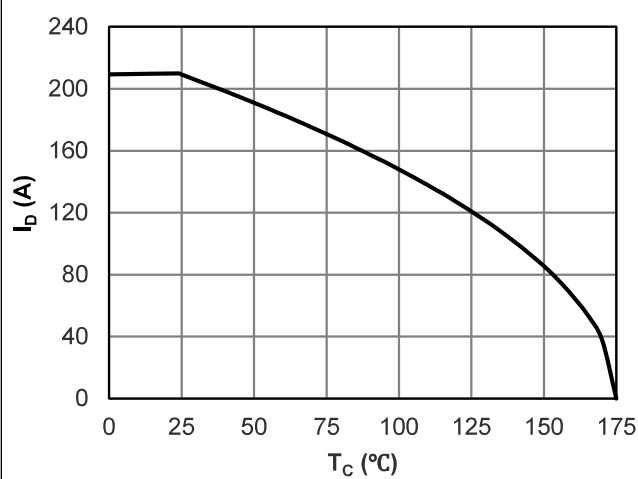


Figure 10: Power De-rating

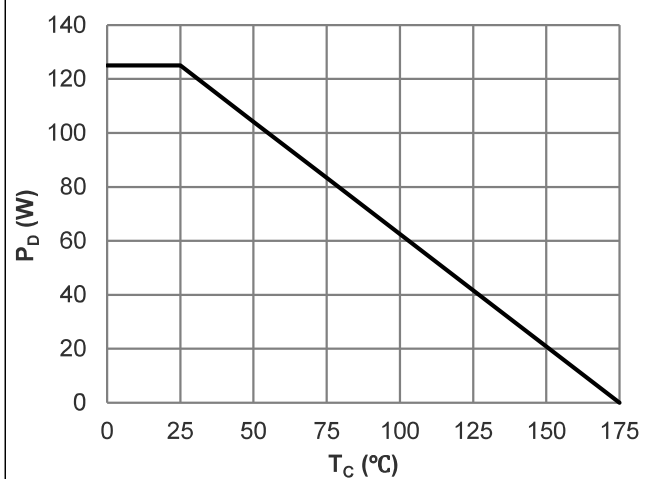


Figure 11: Maximum Safe Operating Area

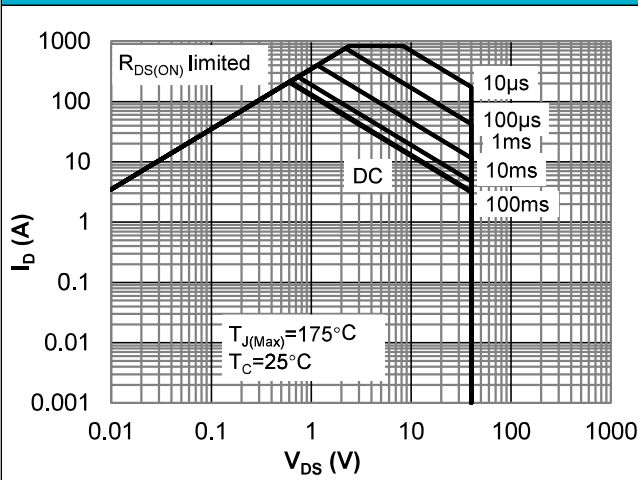
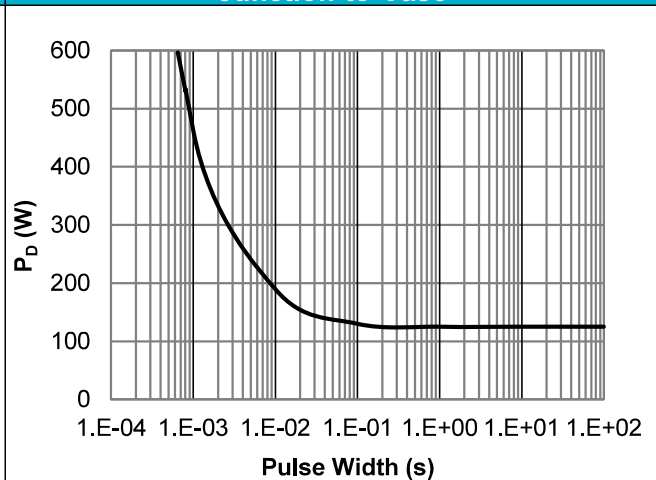
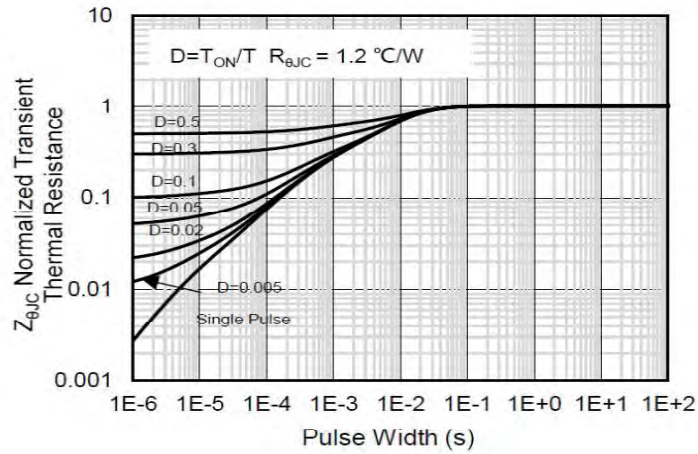


Figure 12: Single Pulse Power Rating, Junction-to-Case



Typical Electrical and Thermal Characteristics

Figure 13: Normalized Maximum Transient Thermal Impedance



Test Circuit

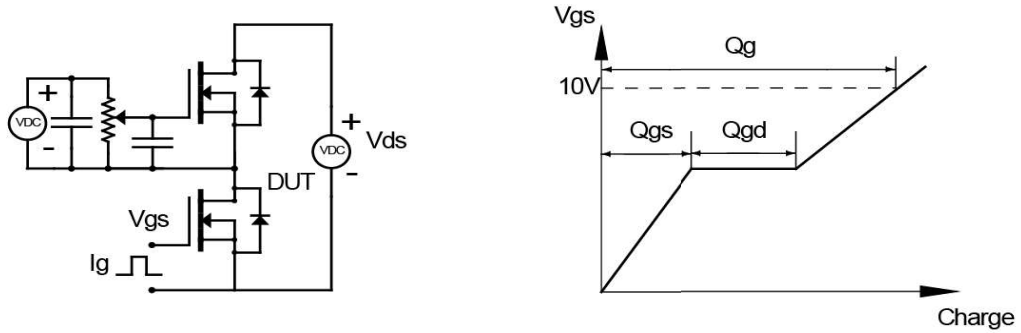


Figure1: Gate Charge Test Circuit & Waveforms

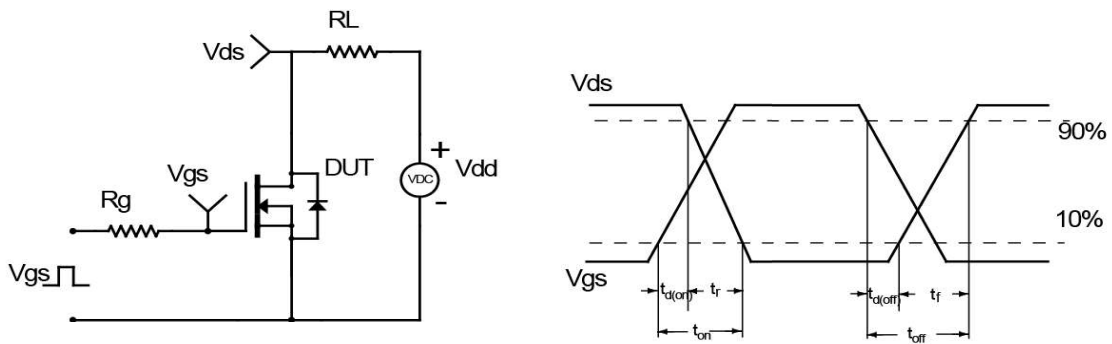


Figure2: Resistive Switching Test Circuit & Waveforms

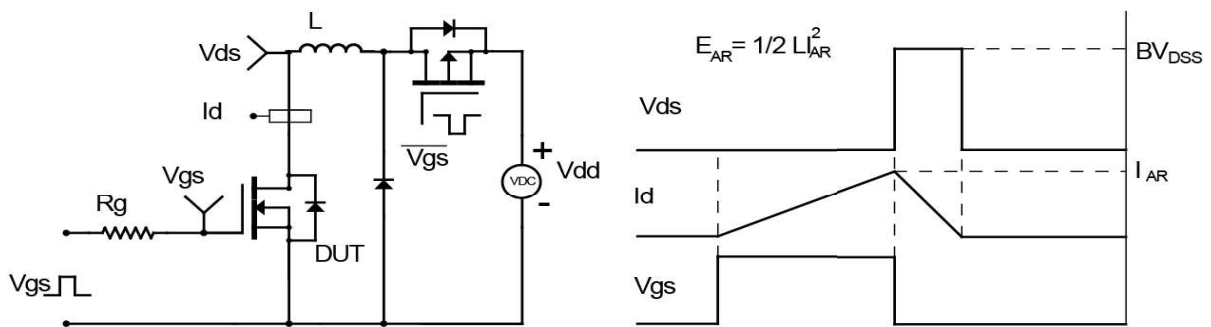


Figure3: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

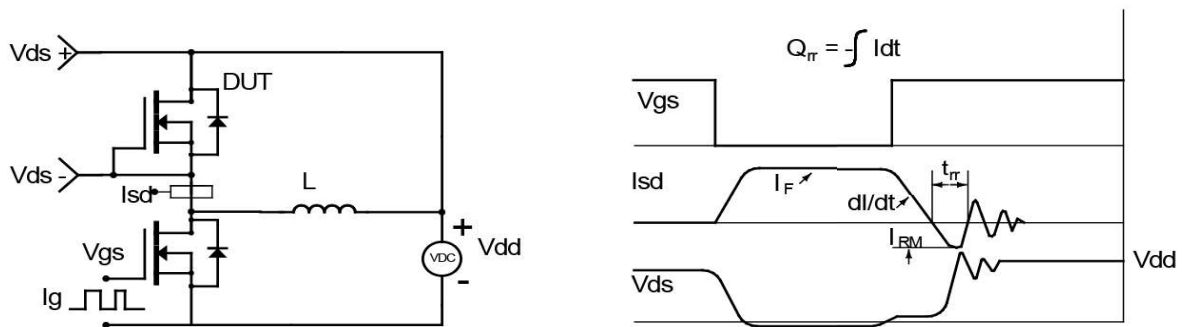
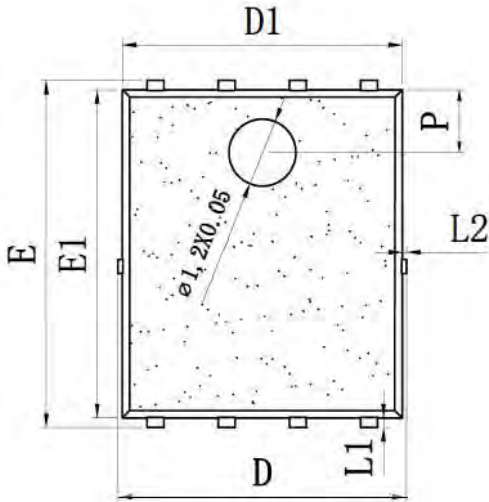
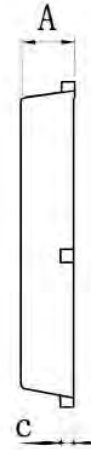


Figure4: Diode Recovery Test Circuit & Waveforms

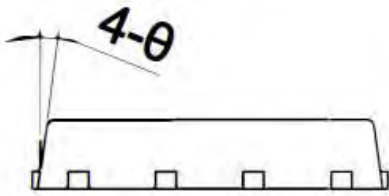
PDFN5x6-8L Package Information



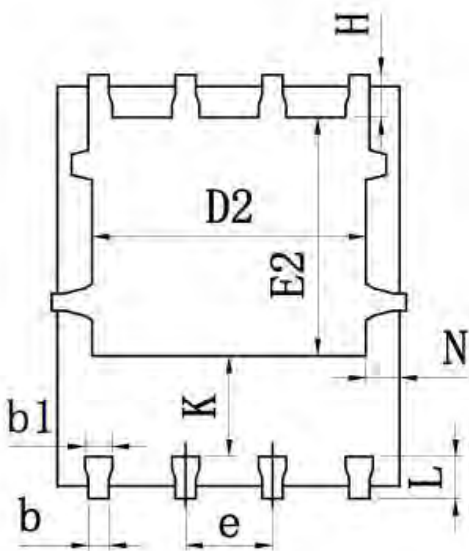
TOP VIEW



SIDE VIEW



SIDE VIEW



BOTTOM VIEW

SYMBOL	mm		
	MIN	NOM	MAX
*A	0.95	1.00	1.05
*b	0.25	0.30	0.35
*b1	0.30	0.40	0.50
*c	0.20	0.25	0.30
D	5.15BSC		
*D1	4.90	5.00	5.10
D2	3.90	4.01	4.20
*e	1.17	1.27	1.37
E	6.15BSC		
*E1	5.75	5.85	5.95
E2	3.35	3.50	3.65
H	0.51	0.61	0.71
K	1.10	1.35	1.50
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2	-	-	0.12
N	0.40	0.50	0.60
P	0.95	1.10	1.25
θ	9°	11°	13°