

30V N-Channel MOSFET

General Description

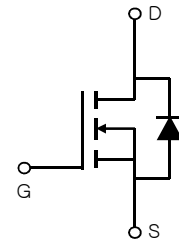
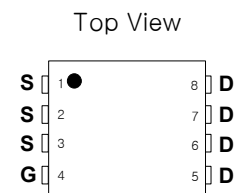
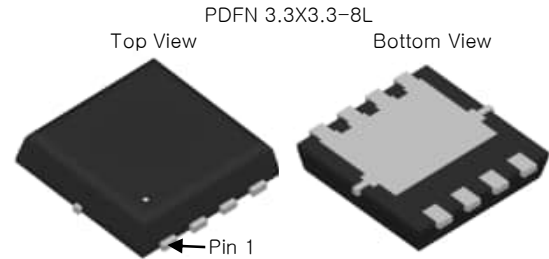
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge

Features

- 30V, 52A
- $R_{DS(ON)}$ Typ = 4.1m Ω @ $V_{GS} = 10V$
- $R_{DS(ON)}$ Typ = 6.2m Ω @ $V_{GS} = 4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

- Load Switch
- PWM Application
- Power Management



Absolute Maximum Ratings (@ $T_C = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	52
		$T_C = 100^\circ C$	31.2
I_{DM}	Pulsed Drain Current ⁽¹⁾	208	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	72	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	35
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	43	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.6	
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ C$

**30V N-Channel MOSFET****Electrical Characteristics** ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.0	1.4	2.5	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10\text{V}, I_D = 20\text{A}$	-	4.1	5.3	m Ω
		$V_{GS} = 4.5\text{V}, I_D = 10\text{A}$	-	6.2	7.1	m Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 15\text{V},$ $f = 1\text{MHz}$	-	1788	-	pF
C_{oss}	Output Capacitance		-	225	-	pF
C_{rss}	Reverse Transfer Capacitance		-	180	-	pF
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 15\text{V}, I_D = 30\text{A}$	-	34	-	nC
Q_{gs}	Gate Source Charge		-	6.5	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	7.5	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime	$V_{GS} = 10\text{V}, V_{DD} = 15\text{V}$ $I_D = 30\text{A}, R_{GEN} = 3\Omega$	-	7	-	ns
t_r	Turn-On Rise Time		-	14	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	34	-	ns
t_f	Turn-Off Fall Time		-	11	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	52	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	160	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 30\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F = 20\text{A}, di/dt = 100\text{A/us}$	-	10	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	1.7	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting $T_J = 25^\circ\text{C}$, $V_{DD} = 15\text{V}$, $V_G = 10\text{V}$, $R_G = 25\text{ohm}$, $L = 0.5\text{mH}$, $I_{AS} = 16\text{A}$
 3. $R_{\theta JA}$ is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB
 4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.



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Typical Performance Characteristics

Figure 1: Output Characteristics

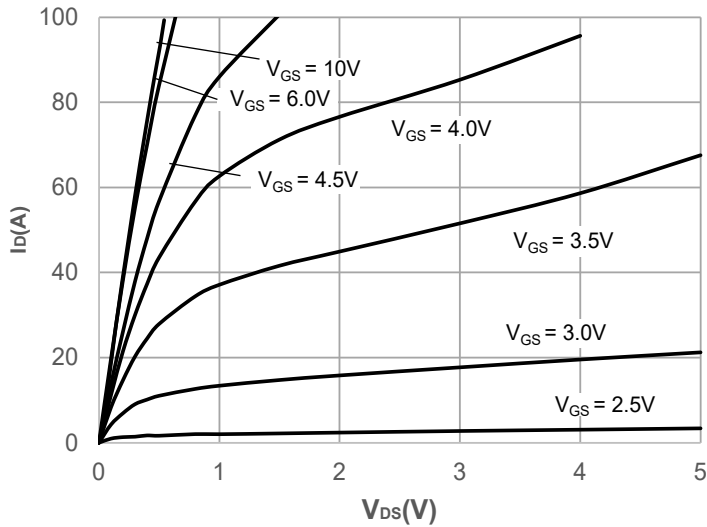


Figure 2: Typical Transfer Characteristics

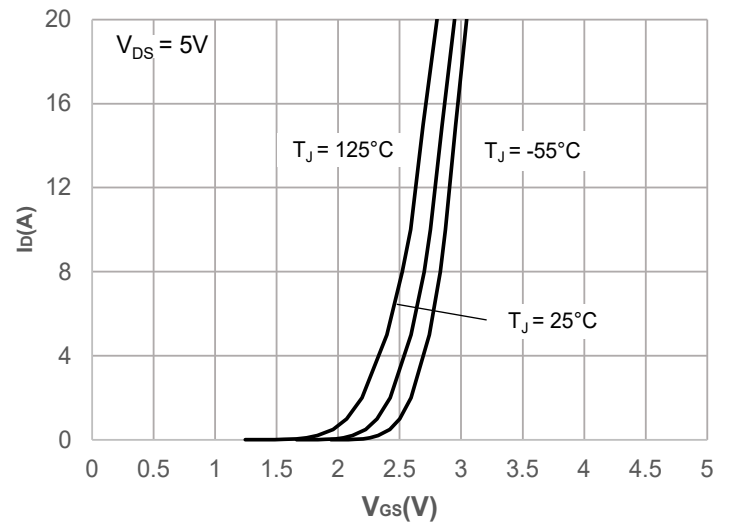


Figure 3: On-resistance vs. Drain Current

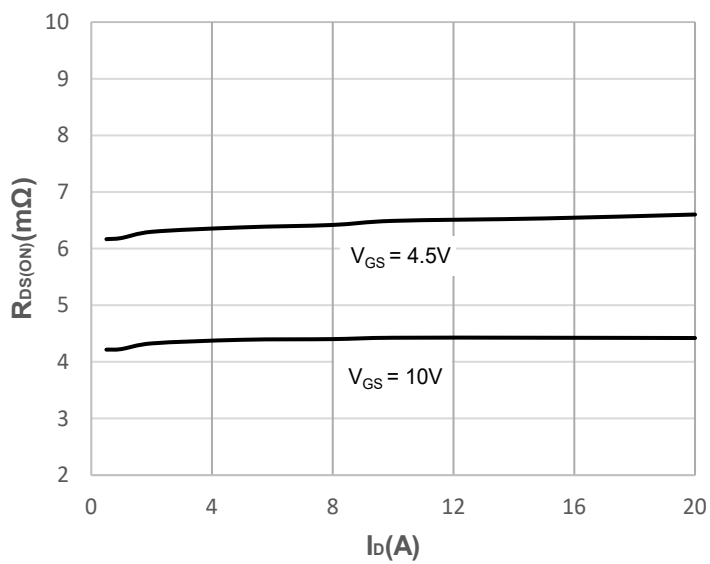


Figure 4: Body Diode Characteristics

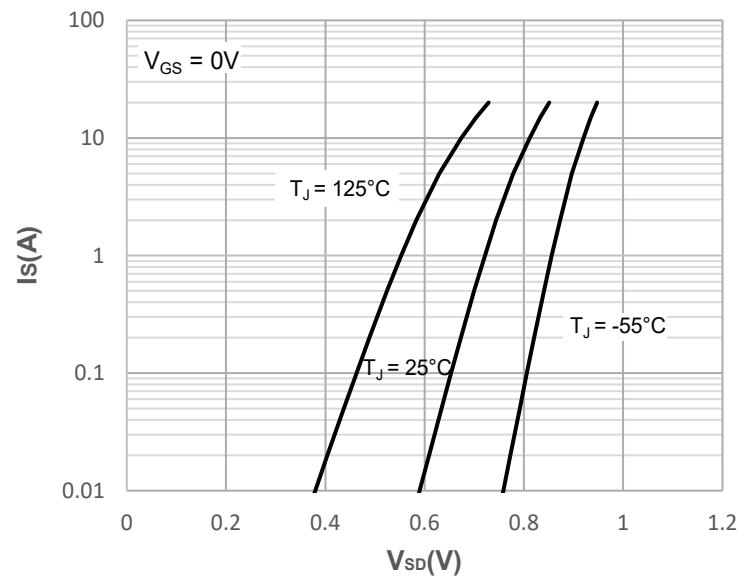


Figure 5: Gate Charge Characteristics

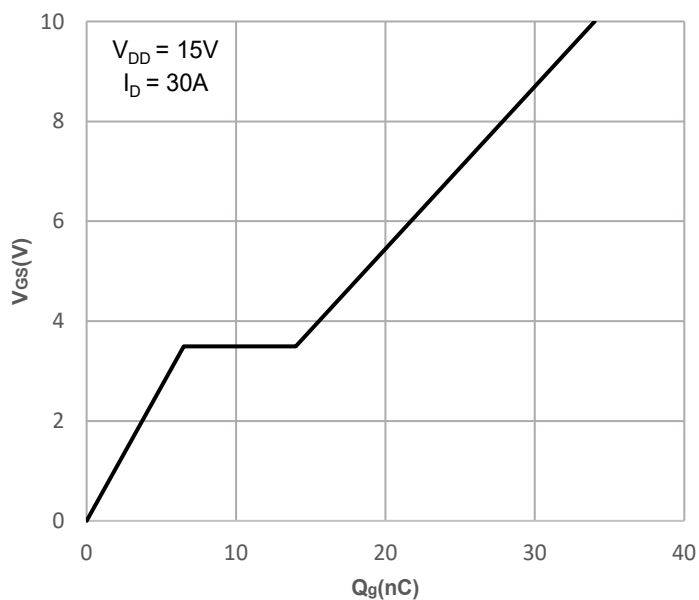
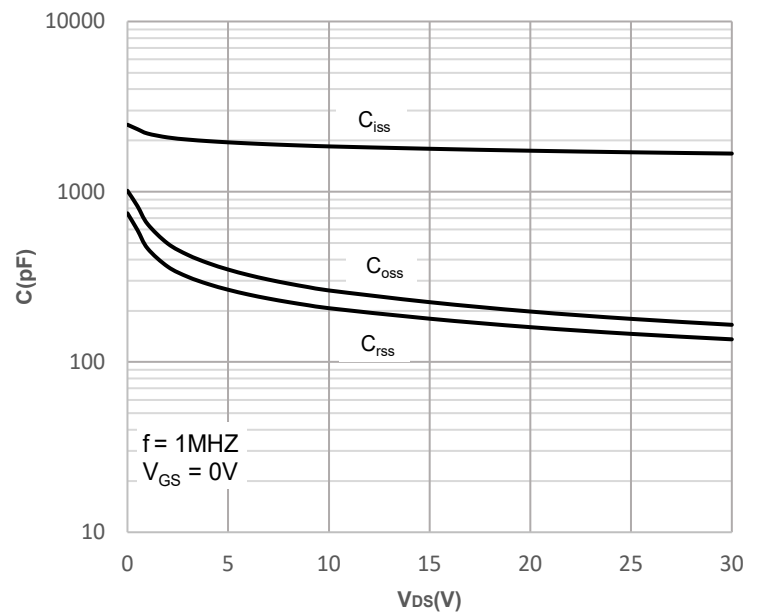


Figure 6: Capacitance Characteristics



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Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

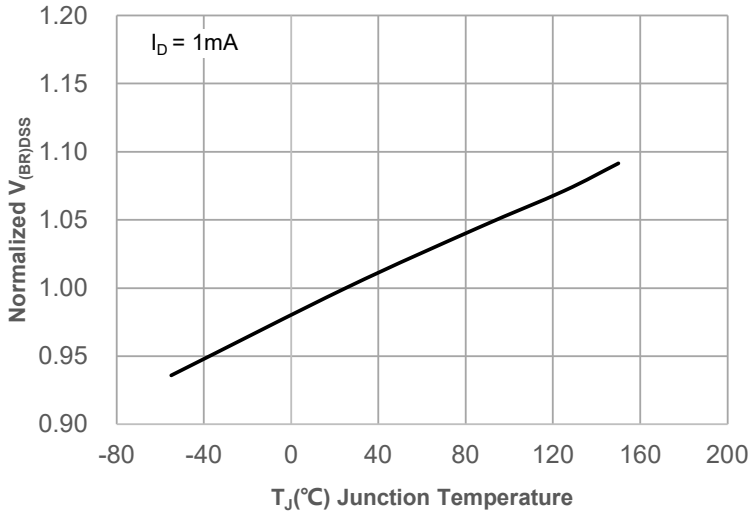


Figure 8: Normalized on Resistance vs. Junction Temperature

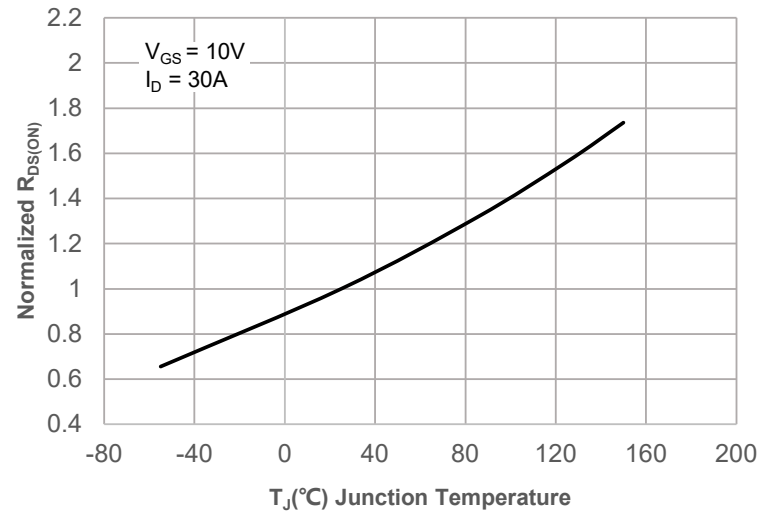


Figure 9: Maximum Safe Operating Area

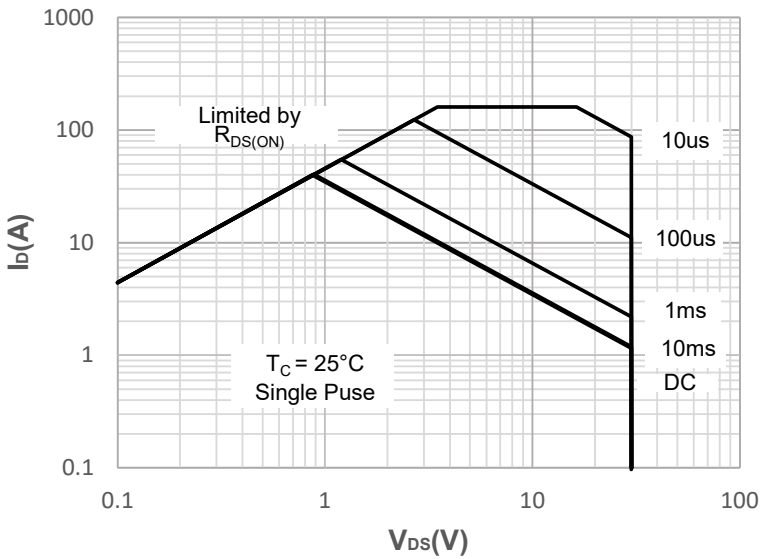


Figure 10: Maximum Continuous Driant Current vs. Case Temperature

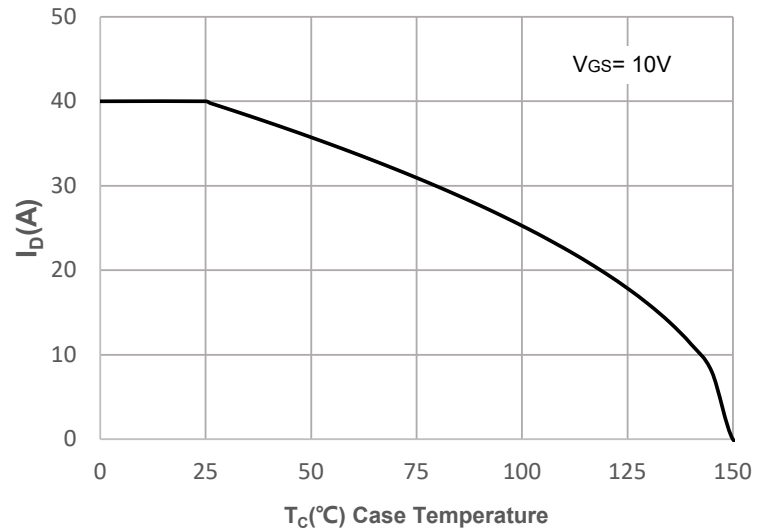


Figure 11: Normalized Maximum Transient Thermal Impedance

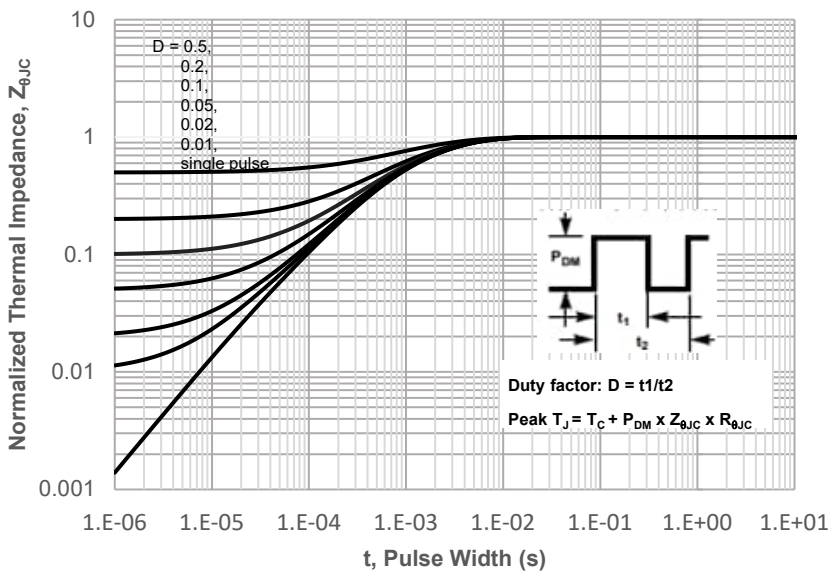
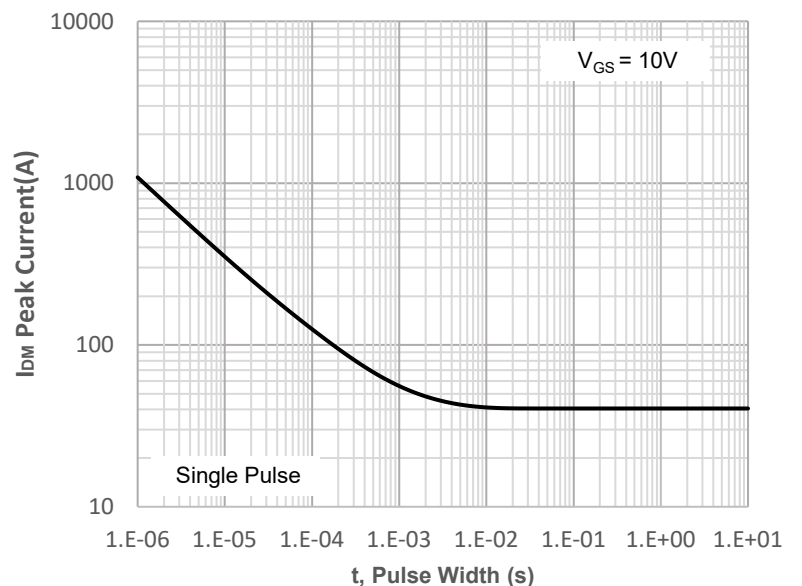


Figure 12: Peak Current Capacity



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Test Circuit

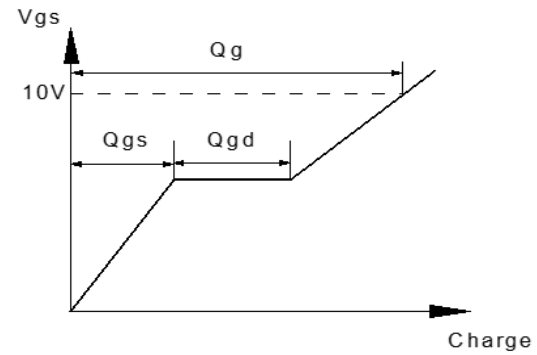
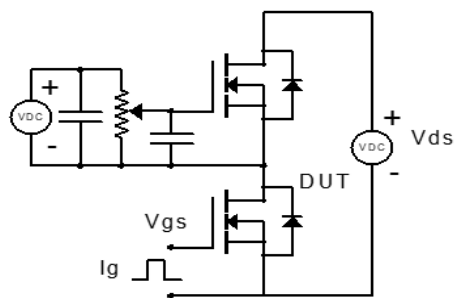


Figure 1: Gate Charge Test Circuit & Waveform

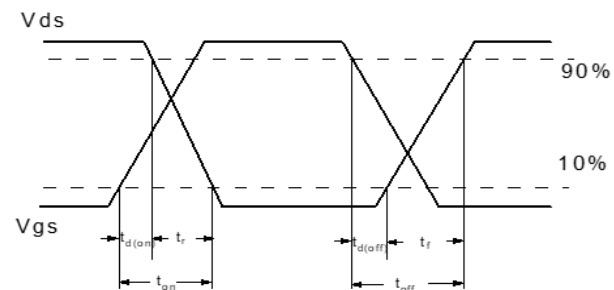
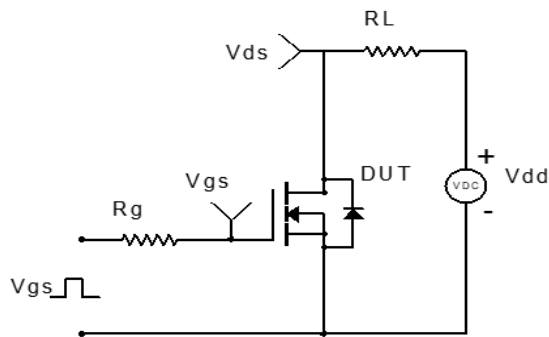


Figure 2: Resistive Switching Test Circuit & Waveform

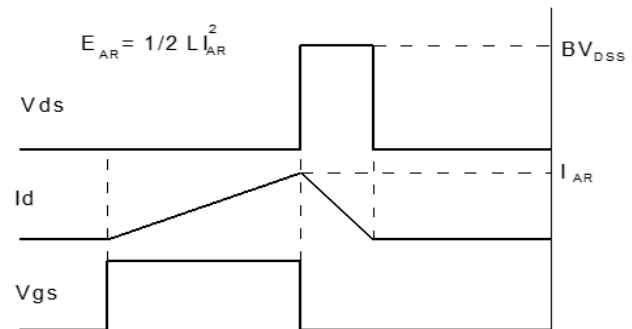
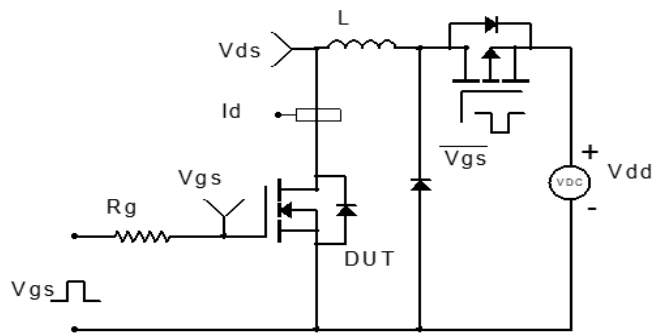


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

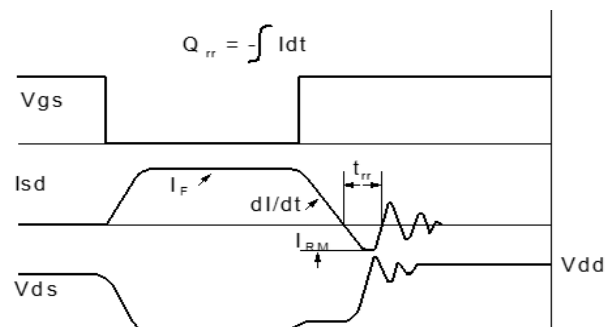
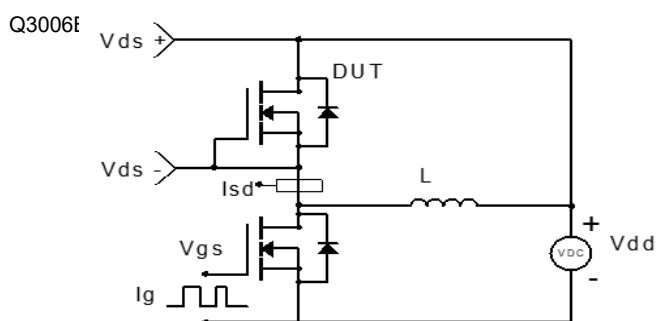
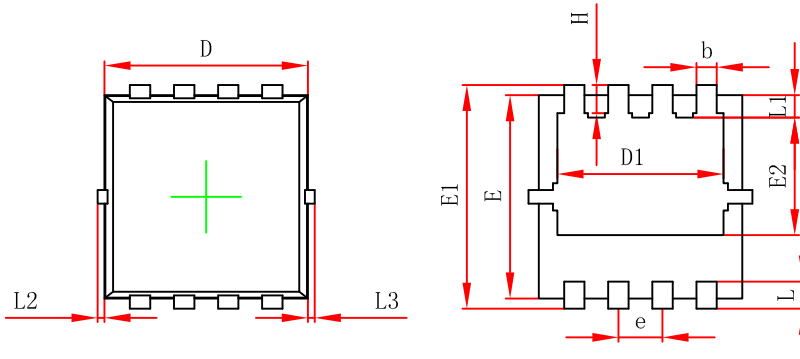


Figure 4: Diode Recovery Test Circuit & Waveform

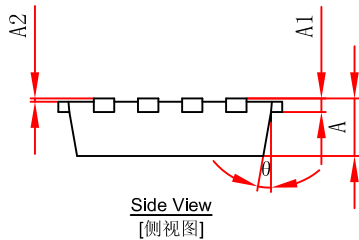
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PDFN 3.3x3.3-8L Package Outline Dimensions



Top View
[顶视图]

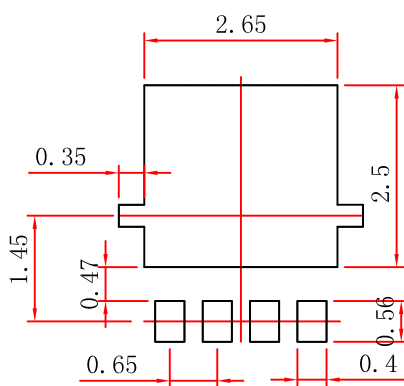
Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

PDFN 3.3x3.3-8L Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.