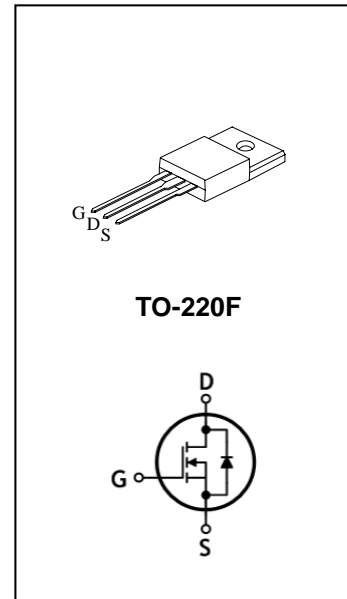


N-CHANNEL POWER MOSFET

● FEATURES

- High Voltage : $BV_{DSS} = 650V(\text{Min.})$
- Low reverse transfer capacitance : $C_{rss} = 14.5pF(\text{Typ.})$
- Low gate charge : $Q_g = 38nC(\text{Typ.})$
- Low drain-source On resistance : $R_{DS(on)} = 0.68\Omega(\text{Typ.})$
- 100% avalanche tested



● Ordering Information

Part No	Package	Packing	Finish	Halogen	Packing Unit
FTK12N65F-A	TO-220F	Tube	Sn	Free	5,000ea

● Maximum Ratings (Tc=25°C, unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	650	V
Gate-source voltage	V_{GSS}	± 30	V
Drain current (DC)*	I_D	Tc = 25 °C	12
		Tc = 100 °C	7.58
Drain current (Pulsed)*	I_{DM}	48	A
Power Dissipation – TO-220F	P_D	50	W
Avalanche current (Single) (Note 2)	I_{AS}	12	A
Single pulsed avalanche energy (Note 2)	E_{AS}	140	mJ
Avalanche current (Repetitive) (Note 1)	I_{AR}	12	A
Repetitive avalanche energy (Note 1)	E_{AR}	7.6	mJ
Junction temperature	T_J	150	°C
Storage temperature range	T_{stg}	-55~150	

*Limited only maximum junction temperature



FTK12N65F-A

● Thermal Characteristic

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 2.7	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

● Electrical Characteristics ($T_C=25^\circ\text{C}$, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D = 250\mu\text{A}$, $V_{DS} = V_{GS}$	3	-	5	V
Drain-source cut-off current	I_{DSS}	$V_{DS} = 650\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
Gate leakage current	I_{GSS}	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance (Note 4)	$R_{DS(ON)}$	$V_{GS} = 10\text{V}$, $I_D = 6.0\text{A}$	-	0.68	0.80	Ω
Forward transfer conductance (Note 4)	g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 6.0\text{A}$	-	13.5	-	S
Input capacitance	C_{iss}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$	-	2470	2882	pF
Output capacitance	C_{oss}		-	160	-	
Reverse transfer capacitance	C_{rss}		-	14.5	-	
Turn-on delay time (Note 3,4)	$T_{d(on)}$	$V_{DS} = 300\text{V}$, $I_D = 12\text{A}$, $R_G = 25\Omega$	-	38	-	ns
Rise time (Note 3,4)	T_r		-	95	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	155	-	
Fall time (Note 3,4)	t_f		-	105	-	
Total gate charge (Note 3,4)	Q_g	$V_{DS} = 520\text{V}$, $V_{GS} = 10\text{V}$, $I_D = 12\text{A}$	-	38	45	nC
Gate-source charge (Note 3,4)	Q_{gs}		-	15	-	
Gate-drain charge (Note 3,4)	Q_g		-	9	-	

● Source-Drain Diode Ratings and Characteristics ($T_C=25^\circ\text{C}$, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	12	A
Source current (Pulsed) (Note 1)	I_{SM}		-	-	48	A
Forward voltage (Note 4)	V_{SD}	$V_{GS} = 0\text{V}$, $I_S = 12\text{A}$	-	-	1.4	V
Reverse recovery time	t_{rr}	$I_S = 12\text{A}$, $V_{GS} = 0\text{V}$	-	500	-	ns
Reverse recovery charge	Q_{rr}	$dI/dt = 100\text{A}/\mu\text{s}$	-	4.3	-	μC

Note :

1. Repetitive rating : Pulse width limited by maximum junction temperature.
2. $L=1.8\text{mH}$, $I_{AS}=12\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature

● Typical Characteristics

Fig. 1 Typical Output Characteristics

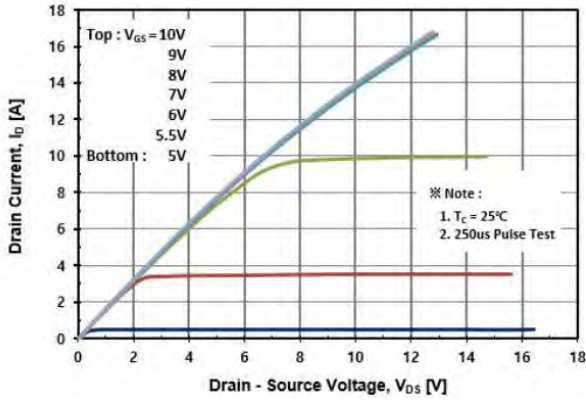


Fig. 2 Typical Output Characteristics

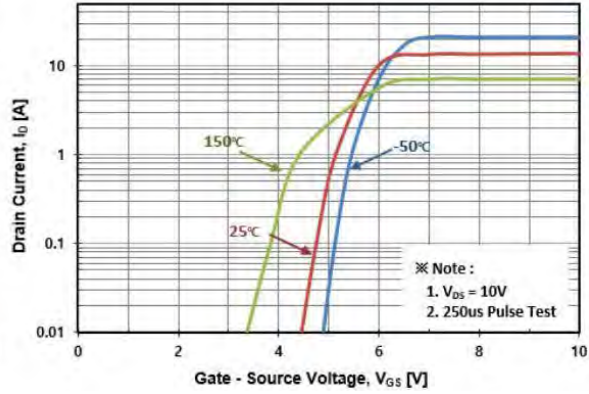


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

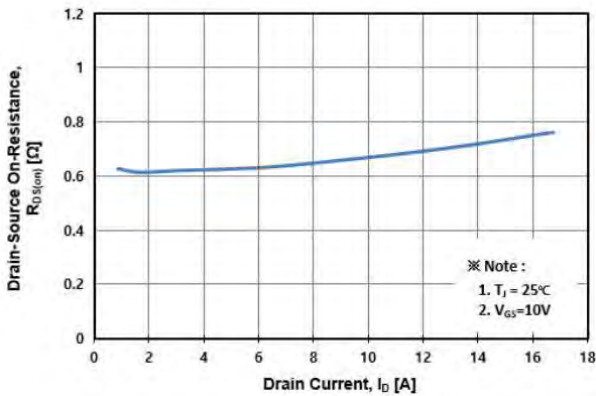


Fig. 4 Body Diode Forward Voltage Variation with Source Current

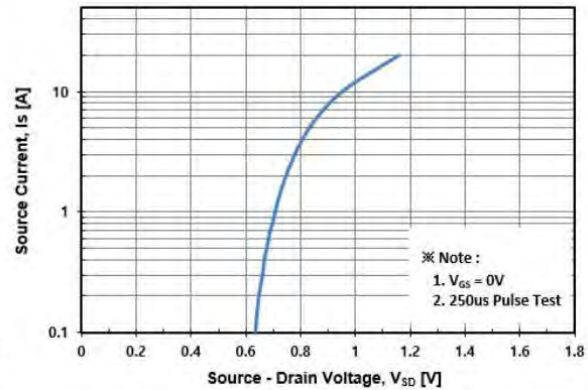


Fig. 5 Typical Capacitance Characteristics

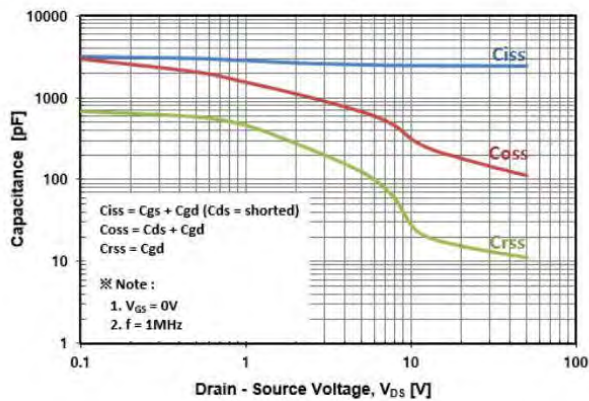
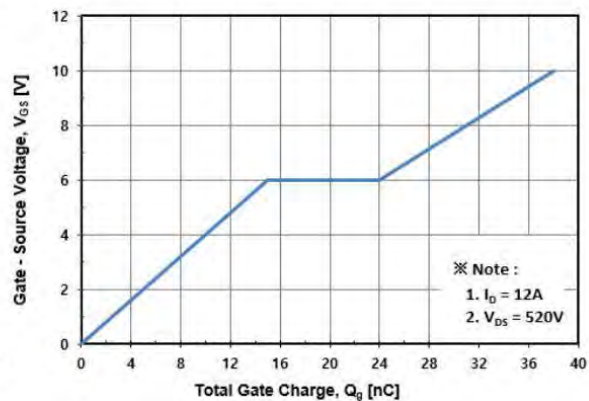


Fig. 6 Typical Total Gate Charge Characteristics



• Typical Characteristics

Fig. 7 Breakdown Voltage Variation vs. Temperature

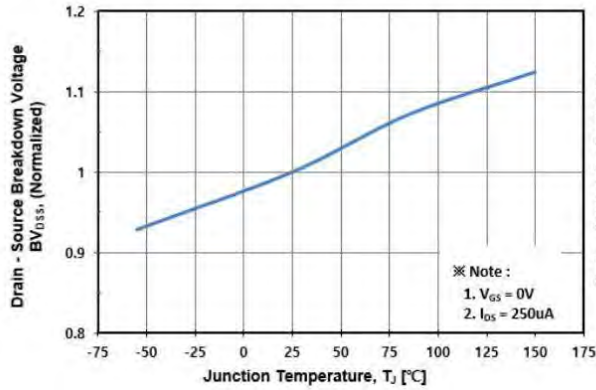


Fig. 8 On-Resistance Variation vs. Temperature

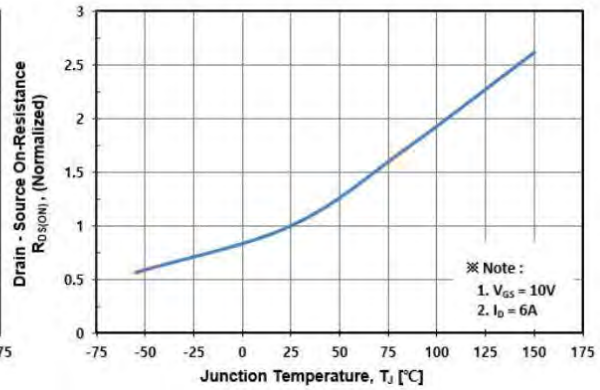


Fig. 9 Maximum Drain Current vs. Case Temperature

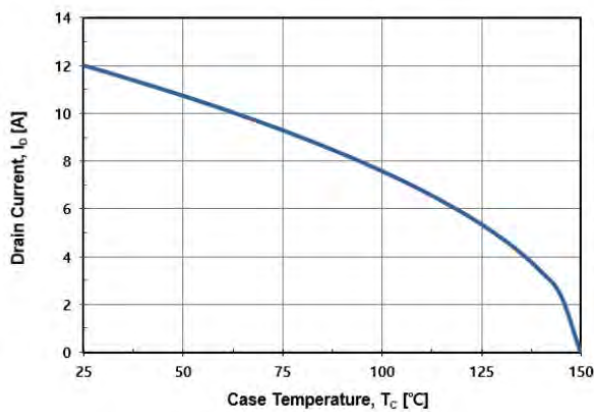


Fig. 10 Maximum Safe Operating Area

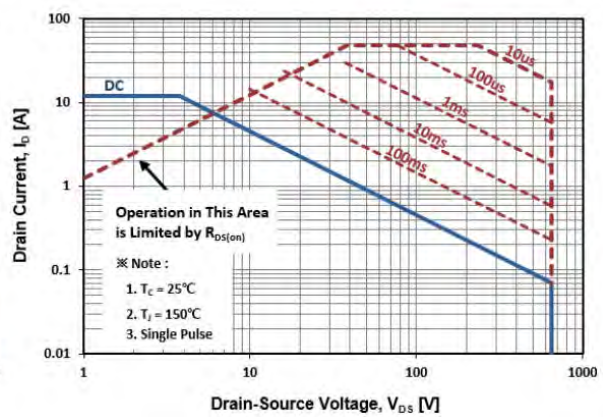


Fig. 11 Transient Thermal Impedance

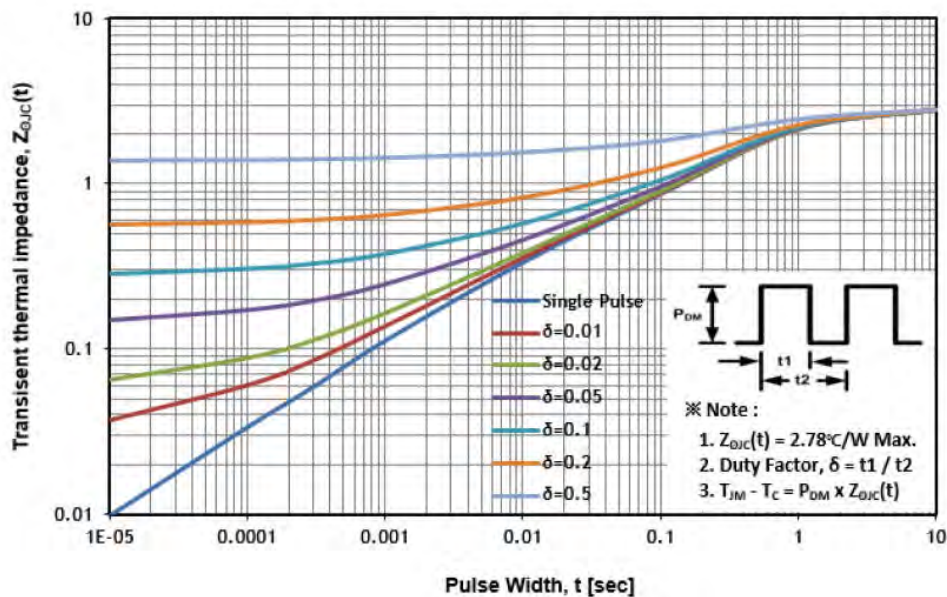


Fig. 12 Gate Charge Test Circuit & Waveform

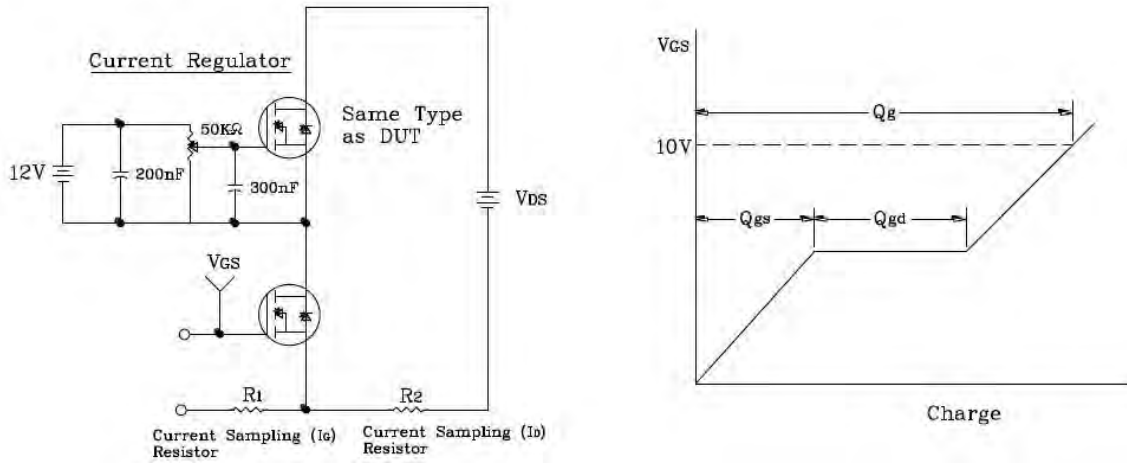


Fig. 13 Resistive Switching Test Circuit & Waveform

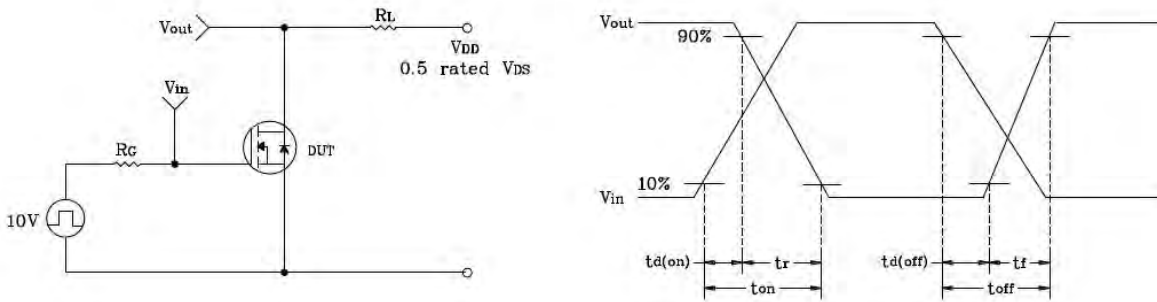


Fig. 14 EAS Test Circuit & Waveform

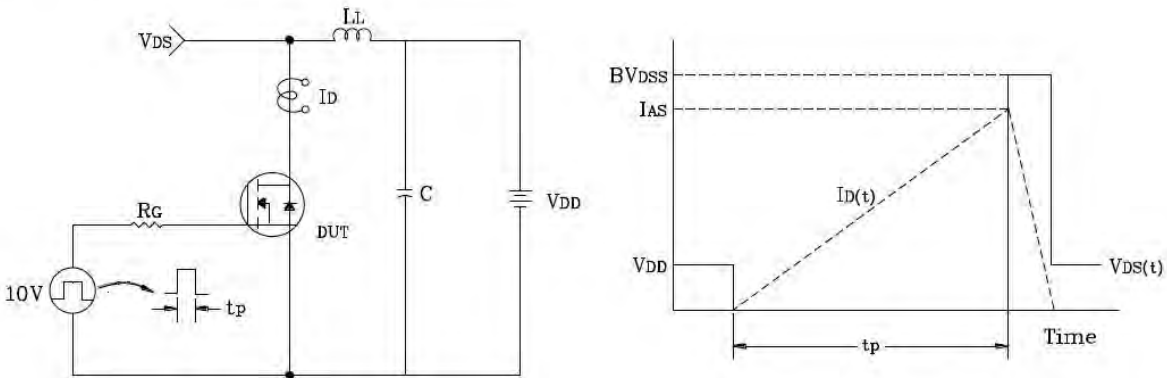


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform

