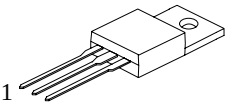
20Amps, 650Volts N-Channel Super Juction MOS-FET

Product Summary

V_{DS} @ $T_{j,max}$	650V
$R_{DS(on),max}$	0.24Ω
I_{DM}	80A
$Q_{g,typ}$	38nC

P :



TO-220

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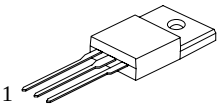

TO-220F

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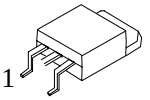


TO-263

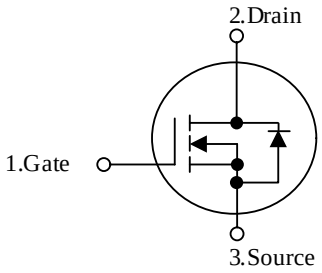
DESCRIPTION

FTK20NS65 Power MOS FET is fabricated using advanced super junction technology. The resulting device has extremely low on resistance, making it especially suitable for applications which require superior power density and outstanding efficiency.

FEATURES

- □ Ultra fast body diode
- □ Ultra low $R_{DS(on)}$
- □ Ultra low gate charge (typ. Q_g = 38nC)
- □ 100% UIS tested
- □ RoHS compliant

SYMBOL



Applications

- □ Power faction correction (PFC).
- □ Switched mode power supplies (SMPS).
- □ Uninterruptible power supply (UPS).

ORDERING INFORMATION

Order Number	Package	Pin Assignment			Packing
		1	2	3	
FTK20NS65P	TO-220	G	D	S	Tube
FTK20NS65F	TO-220F	G	D	S	Tube
FTK20NS65DD	TO-263	G	D	S	Reel & Taping

Note: Pin Assignmen: G: Gate D: Drain S: Source

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DSS}	650	V
Continuous drain current (T_C = 25°C)	I_D	20	A
(T_C = 100°C)		12	A
Pulsed drain current	I_{DM}	80	A
Gate - Source voltage	V_{GSS}	± 30	V
Avalanche energy, single pulse [1)]	E_{AS}	806	mJ
Power Dissipation (T_C = 25°C)	P_D	205	W
- Derate above 25°C		1.64	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C
Continuous diode forward current	I_S	20	A
Diode pulse current	$I_{S,pulse}$	80	A

Thermal CharacteristicsTO-220/TO-263

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.55	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

Thermal Characteristics TO-220F

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.9	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

Electrical Characteristics

T_c = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0 V, I_D=0.25 mA	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.25mA	2.0	3.0	4.0	V
Drain cut-off current	I_{DSS}	V_{DS}=650 V, V_{GS}=0 V, T_j = 25°C T_j = 125°C	 - -	 - 10	 1 -	μA
Gate leakage current, Forward	I_{GSSF}	V_{GS}=30 V, V_{DS}=0 V	-	-	100	nA
Gate leakage current, Reverse	I_{GSSR}	V_{GS}=-30 V, V_{DS}=0 V	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=10 A T_j = 25°C T_j = 150°C	- - -	 0.2 0.35	 0.24 -	Ω
Gate resistance	R_G	f=1 MHz, open drain	-	2.2	-	Ω
Dynamic characteristics						
Input capacitance	C_{iss}	V_{DS} = 100 V, V_{GS} = 0V f = 1 MHz	-	1197	-	pF
Output capacitance	C_{oss}		-	67	-	
Reverse transfer capacitance	C_{rss}		-	3.7	-	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 325V, I_D = 20A R_G = 25Ω, V_{GS}=10V 2), 3)	-	20	-	ns
Rise time	t_r		-	56	-	
Turn-off delay time	$t_{d(off)}$		-	106	-	
Fall time	t_f		-	41	-	
Gate charge characteristics						
Gate to source charge	Q_{gs}	V_{DD}=520 V, I_D=20A, V_{GS}=0 to 10 V 2), 3)	-	9.0	-	nC
Gate to drain charge	Q_{gd}		-	20	-	
Gate charge total	Q_g		-	38	-	
Reverse diode characteristics						
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=20A	-		1.4	V
Reverse recovery time	t_{rr}	V_R=50 V, I_F=20A, dI_F/dt=100 A/μs 2)	-	420	-	ns
Reverse recovery charge	Q_{rr}		-	6.1	-	μC

Notes:

1. L=79mH, I_{AS} = 4.2A, V_{DD} =100V, R_G = 250Ω, Starting T_j= 25°C.
2. Pulse Test: Pulse width <300ys,Duty cycles 2%;
3. Essentially independent of operating temperature.

Typical Characteristics

Electrical Characteristics Diagrams

Figure 1. On-Region Characteristics

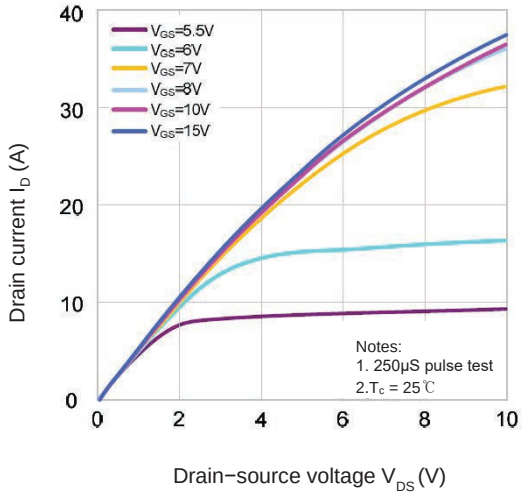


Figure 2. Transfer Characteristics

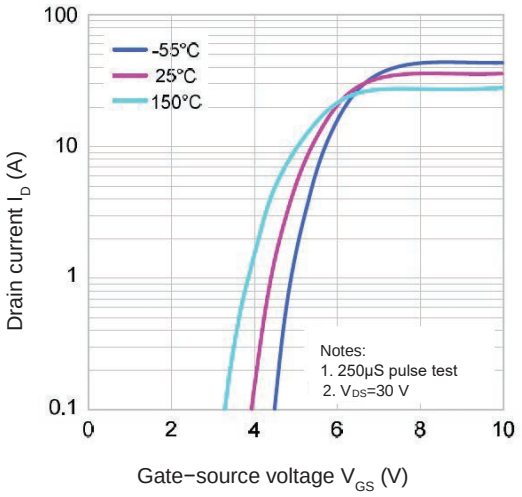


Figure 3. On-Resistance Variation vs. Drain Current

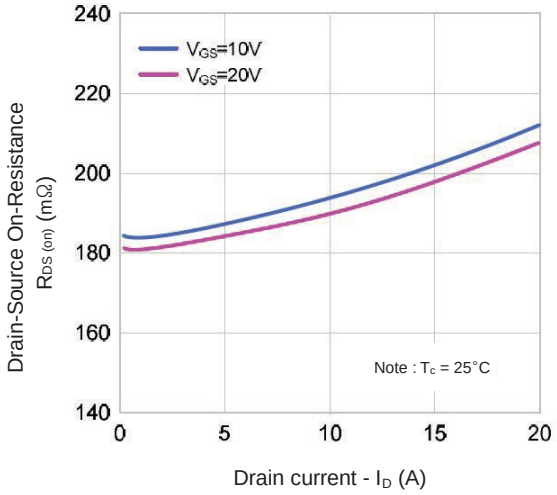


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

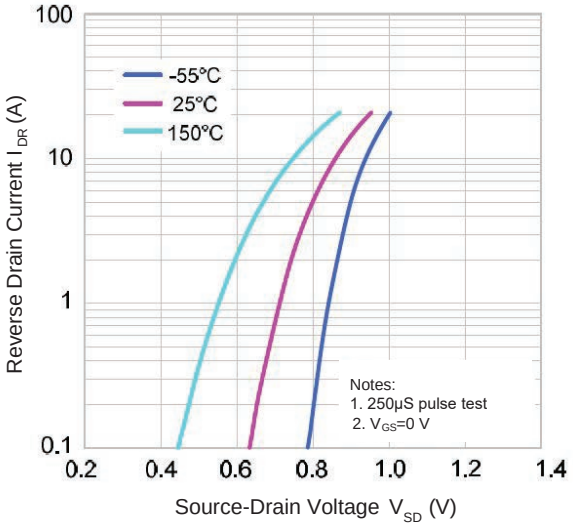


Figure 5. Capacitance Characteristics

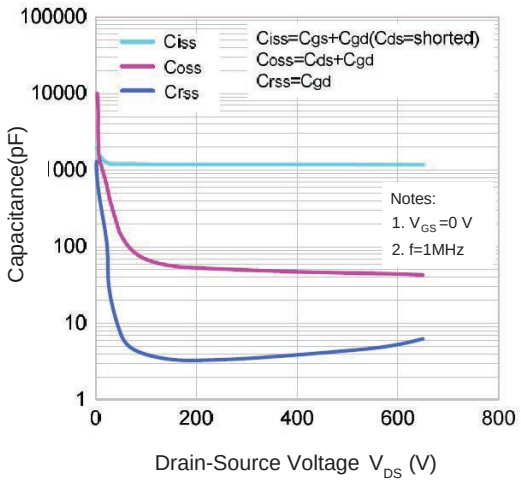


Figure 6. Gate Charge Characteristics

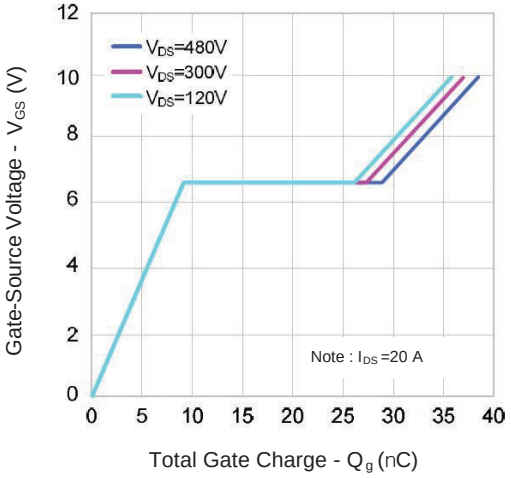


Figure 7. Breakdown Voltage Variation vs. Temperature

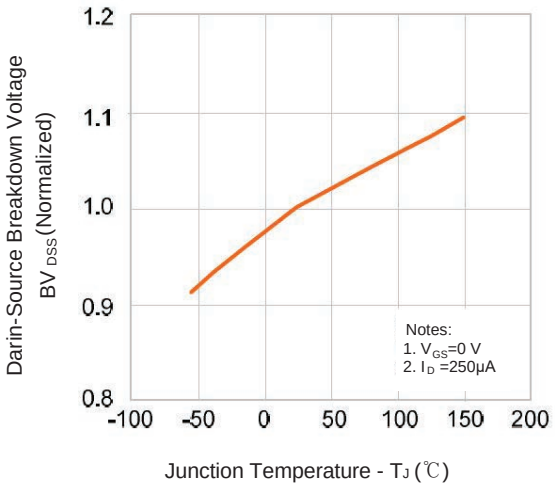


Figure 8. On-resistance Variation vs. Temperature

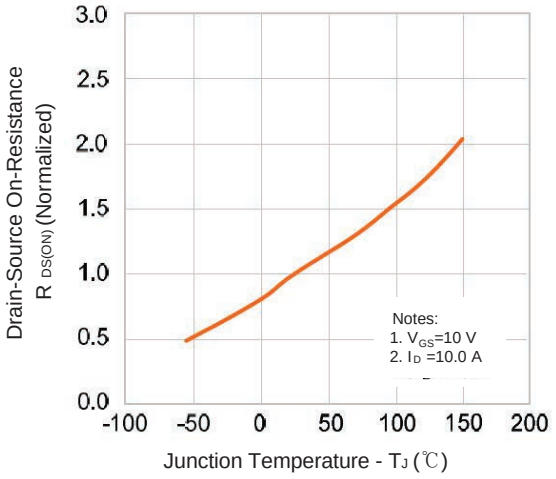


Figure 9.1 Maximum Safe Operating Area (FTK20N65F)

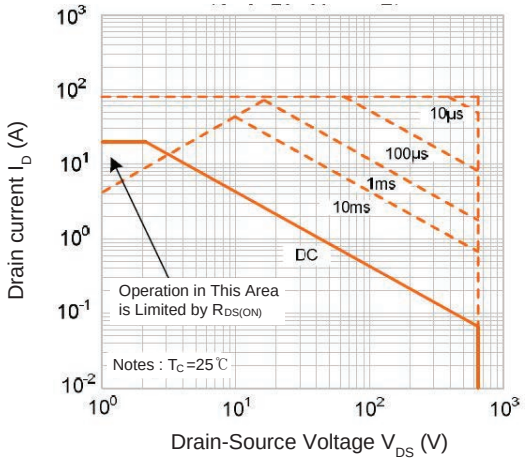
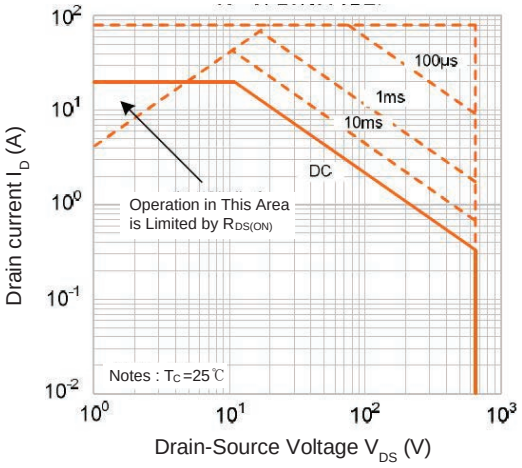


Figure 9.2 Maximum Safe Operating Area (FTK20N65P / FTK20N65DD)



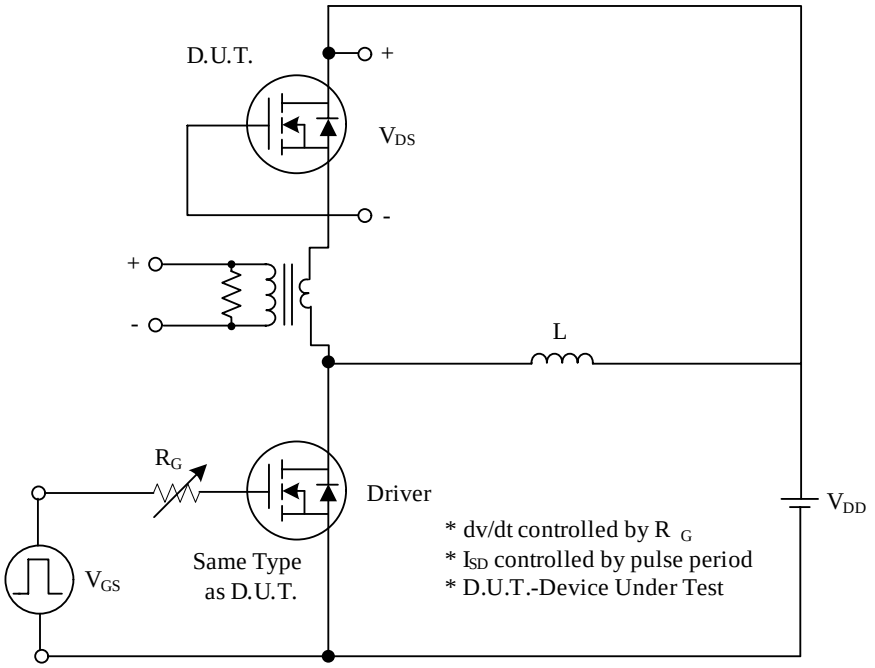


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

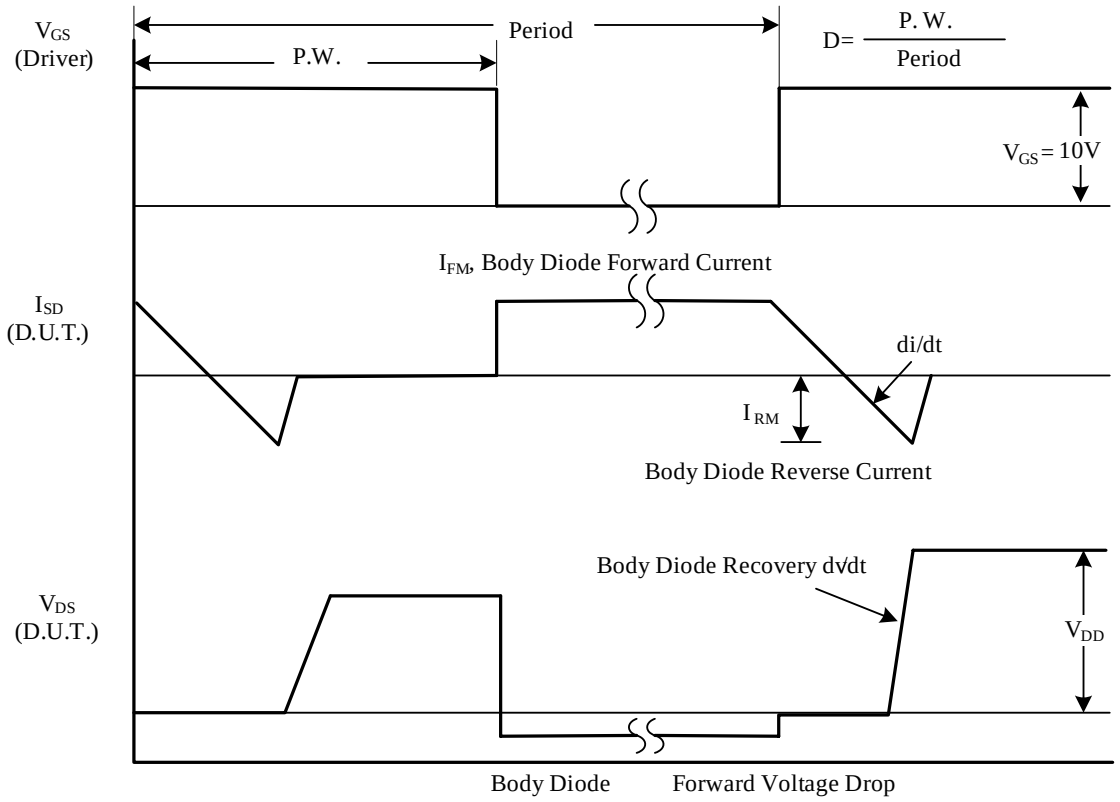


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

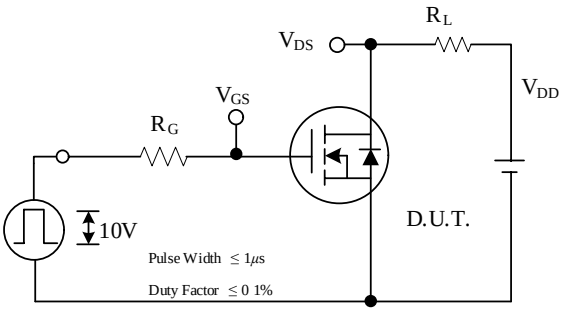


Fig. 2A Switching Test Circuit

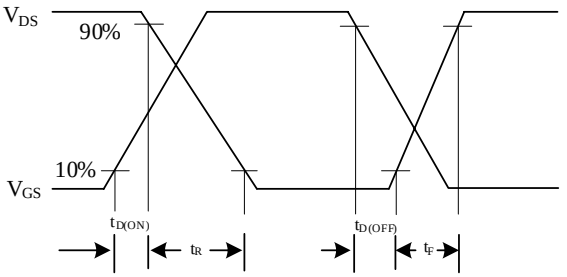


Fig. 2B Switching Waveforms

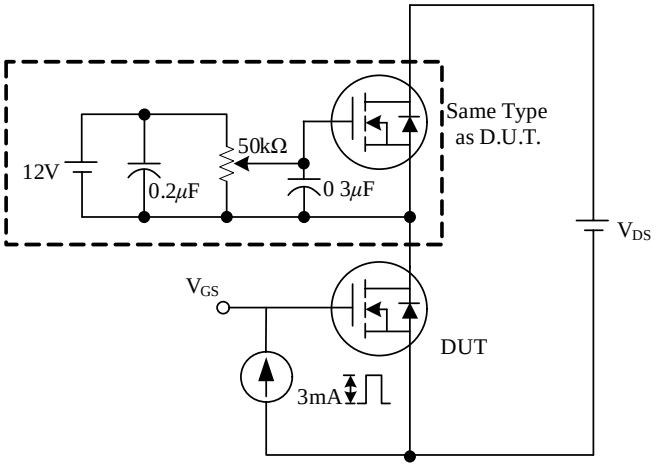


Fig. 3A Gate Charge Test Circuit

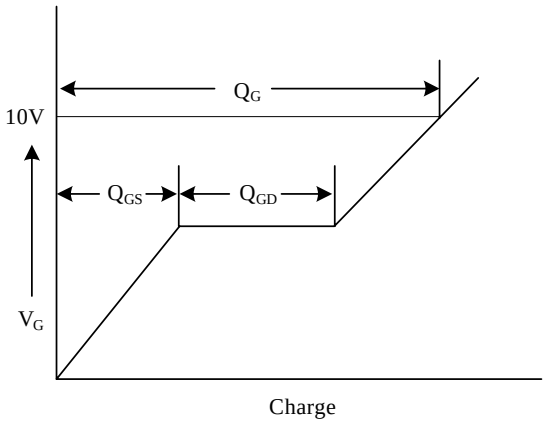


Fig. 3B Gate Charge Waveform

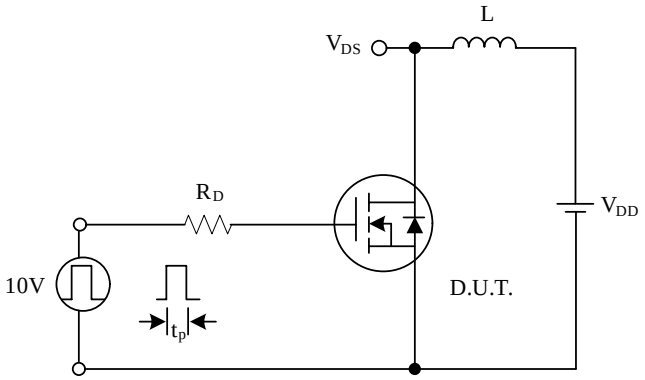


Fig. 4A Unclamped Inductive Switching Test Circuit

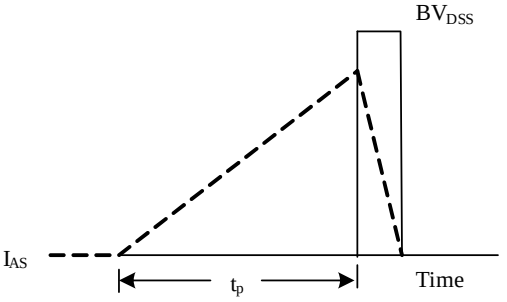


Fig. 4B Unclamped Inductive Switching Waveforms