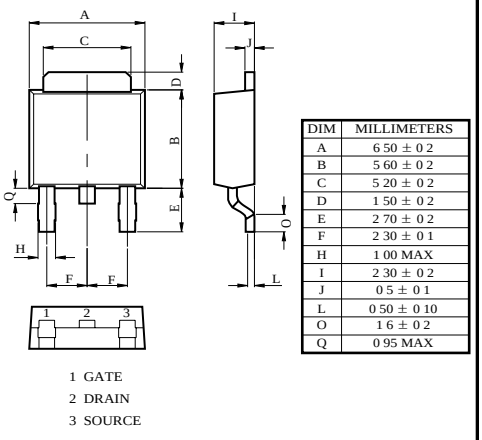
650V N-Channel S/J MOSFET

Main Product Characteristics:

$V_{(BR)DSS}$	650V
$R_{DS(ON)}$	0.78Ω(typ.)
I_D	5A

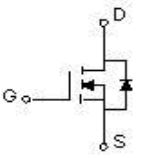


DIM	MILLIMETERS
A	6 50 ± 0 2
B	5 60 ± 0 2
C	5 20 ± 0 2
D	1 50 ± 0 2
E	2 70 ± 0 2
F	2 30 ± 0 1
H	1 00 MAX
I	2 30 ± 0 2
J	0 5 ± 0 1
L	0 50 ± 0 10
O	1 6 ± 0 2
Q	0 95 MAX

D-PAK (TO-252)

Features and Benefits

- Grand Turbo MOSFET process technology.
- Optimized the cell structure.
- Low on-resistance and low gate charge.
- Featuring low switching and drive losses.
- Fast switching and reverse body recovery.
- High ruggedness and robustness.



Description

The GT series products utilizes Trust's outstanding standard turbo process and packaging techniques to achieve ultral low on-resistance and low gate charge and to provide the industry's best-in-class performance.

These features make this series products extremely efficient, temperature characteristics and reliable for use in power management, synchronous rectification, battery protection, load switch and a wide variety of other applications.

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter	Symbol	Parameter.	Unit
Drain-Source Voltage	V_{DS}	650	V
Gate-to-Source Voltage	V_{GS}	±30	V
Continuous Drain Current, @ Steady-State	ID @ T_C = 25°C	5	A
Continuous Drain Current, @ Steady-State	ID @ T_C = 100°C	3.2	A
Pulsed Drain Current	I_{DM}	20	A
Power Dissipation	PD @ T_C = 25°C	42	W
		0.34	W/°C
Single Pulse Avalanche Energy[1]	E_{AS}	214	mJ
Single Pulse Avalanche Current	I_{AS}	2.8	A
Body diode reverse voltage slope[2]	dv/dt	15	V/ns
MOS dv/dt reggedness[3]	dv/dt	50	V/ns
Junction-to-Ambient (PCB Mounted, Steady-State)	$R_{\theta JA}$	62.0	°C/W
Junction-to-Case	$R_{\theta JC}$	2.97	°C/W
Operating Junction and Storage Temperature Range	T_J/T_{STG}	-55 to + 150	°C
Soldering temperature	Tsold	260	°C

Electrical Characteristics (T_J=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, ID=250μA	650	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	VDS=650V, VGS=0V, T_J=25℃	-	-	1.0	μA
		VDS=650V, VGS=0V, T_J=125℃	-	1.5	-	μA
Gate-to-Source Forward Leakage	I_{GSS}	VDS=0V,V_{GS}=30V	-	-	100	nA
		VDS=0V,V_{GS}= -30V	-	-	-100	
Static Drain-to-Source On- Resitance	$R_{DS\ (on)}$	V_{GS}=10V, ID=2.5A	-	0.78	0.90	Ω
Gate Threshold Voltage	$V_{GS\ (th)}$	V_{DS}=V_{GS}, I_D=250μA	2.0	-	4.0	V
Gate Resistance	Rg	f=1MHz	-	7.2	-	Ω
Input Capacitance	Ciss	V_{GS}=0V V_{DS}=100V,*f*=1MHz	-	300	-	pF
Output Capacitance	Coss		-	20	-	
Reverse transfer capacitance	Crss		-	2.4	-	
Total Gate Charge [4,5]	Qg	I_D=5A, V_{DD}=520V,V_{GS}=10V	-	13	-	nC
Gate-to-Source Charge [4,5]	Qgs		-	3.0	-	
Gate-to-Drain("Miller") Charge[4,5]	Qgd		-	6.8	-	
Gate Plateau[4,5]	Vplateau		-	6.5	-	V
Turn-on Delay Time[4,5]	td(on)	V_{DD}=325V, V_{GS}=10V, R_G=24Ω,ID=5A	-	8.7	-	nS
Rise Time[4,5]	tr		-	25	-	
Turn-Off Delay Time[4,5]	td(off)		-	30	-	
Fall Time[4,5]	tf		-	23	-	
Source-Drain Ratings and Characteristics						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Continuous Source Current (Body Diode)	I_S	T_C=25°C,MOSFETsymbol showing the integral reverse p-n junction diode.	-	-	5	A
Diode Pulse Current	$I_{S,pulse}$		-	-	20	A
Diode Forward Voltage	V_{SD}	I_S=5A, V_{GS}=0V	-	-	1.4	V
Reverse Recovery Time [4]	t_{rr}	I_s=5A,V_{GS}=0V, dIF/dt=100A/us	-	334	-	nS
Reverse Recovery Charge [4]	Q_{rr}		-	2.2	-	μC

Notes:

1. L=79㎜H,V_{DD}=100V, R_G=25Ω, starting temperature T_J=25°C .
2. V_{DS}=0~400V, I_{SD}<=I_S, T_J=25°C .
3. V_{DS}=0~480V.
4. Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
5. Essentially Independent of Operating Temperature.

Typical Electrical and Thermal Characteristic Curves

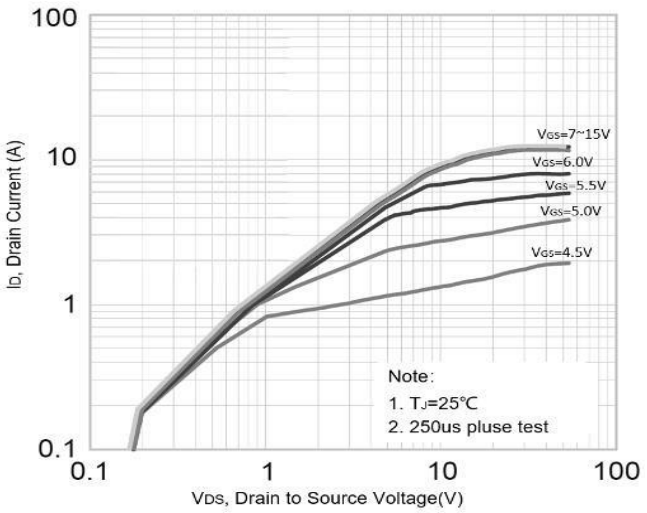


Figure1. Typical Output Characteristics

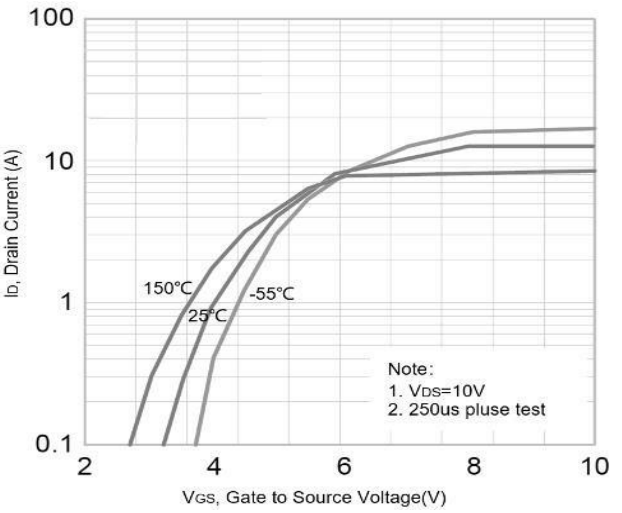


Figure2. Transfer Characteristics

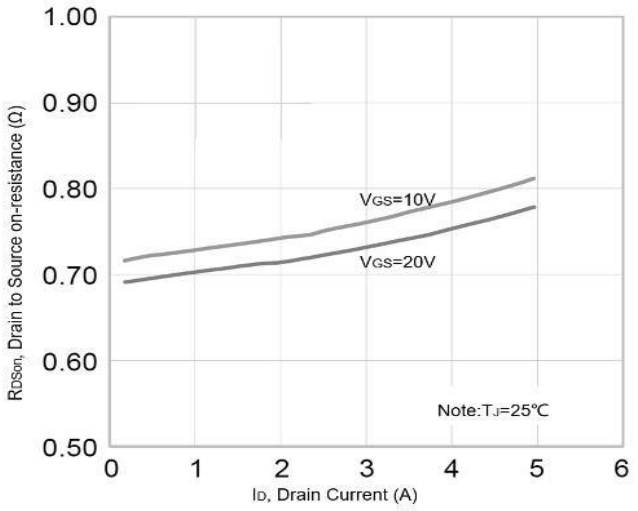


Figure3. Rdson vs. Drain Current

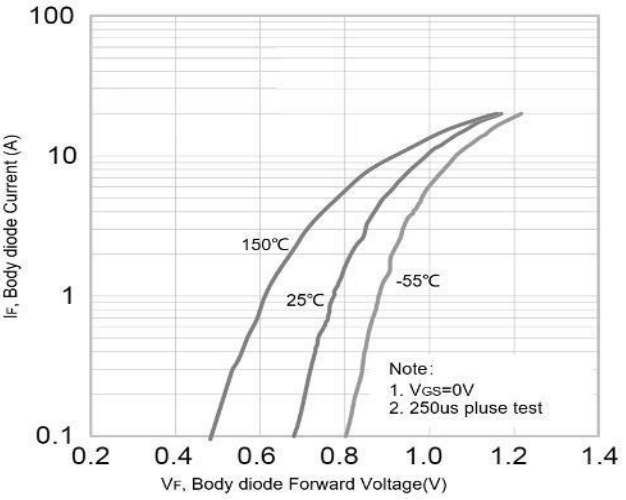


Figure4. Body Diode Characteristic

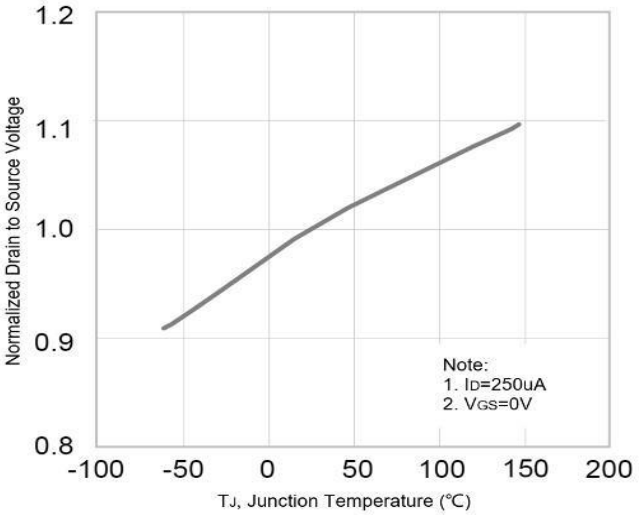


Figure5. Normalized BVdss vs.T_J

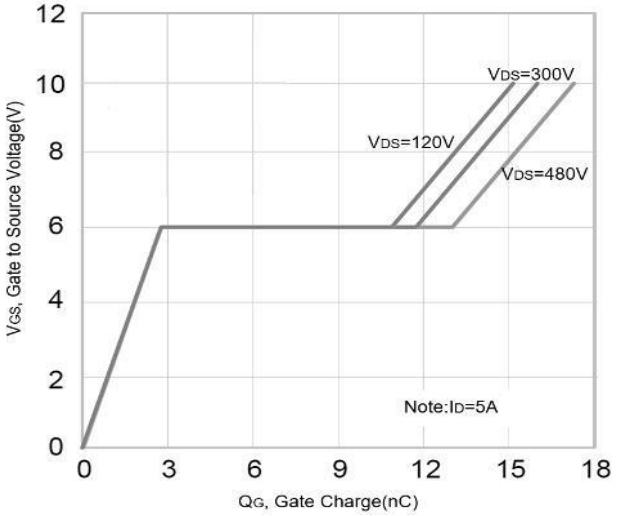


Figure6. Gate Charge Characteristic

Typical Electrical and Thermal Characteristic Curves

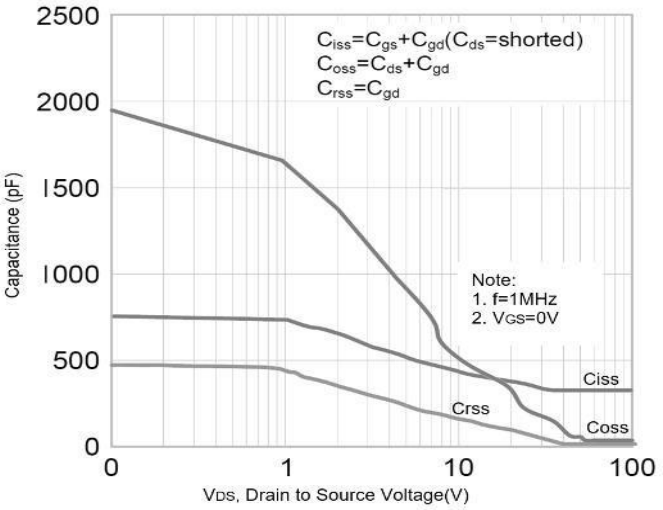


Figure7 Capacitance Characteristic

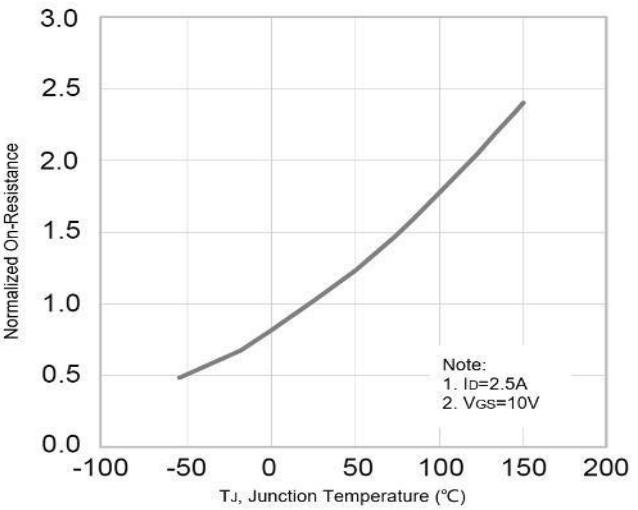


Figure8 Normalized Rdson vs.T_J

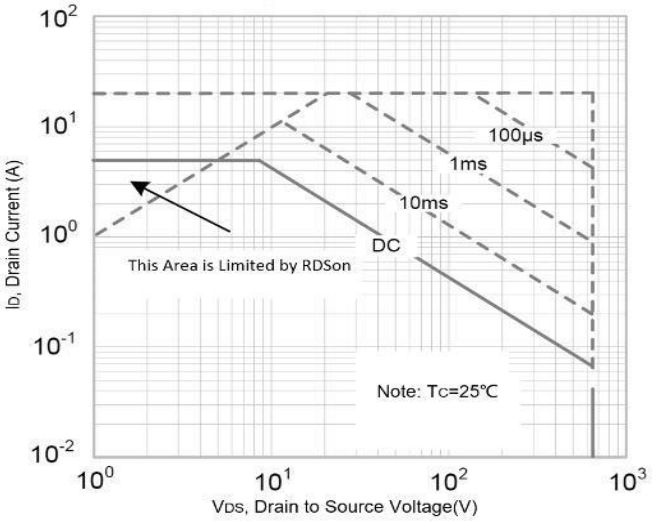


Figure9. Safe Operation Area

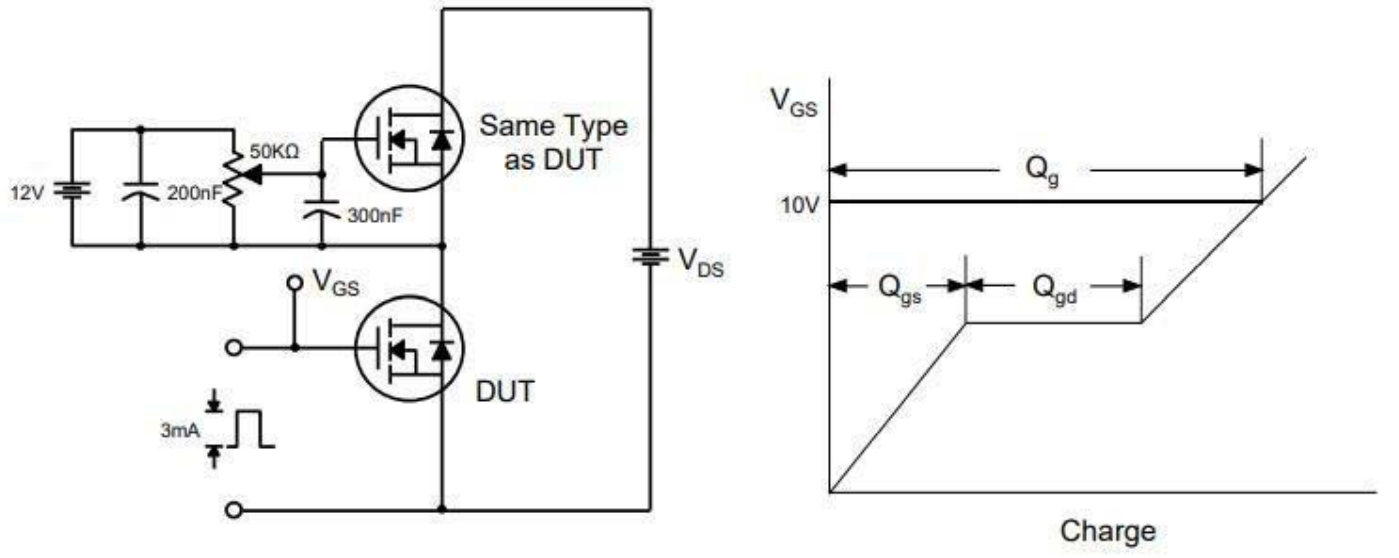


Figure 10. Gate Charge Test Circuit & Waveforms

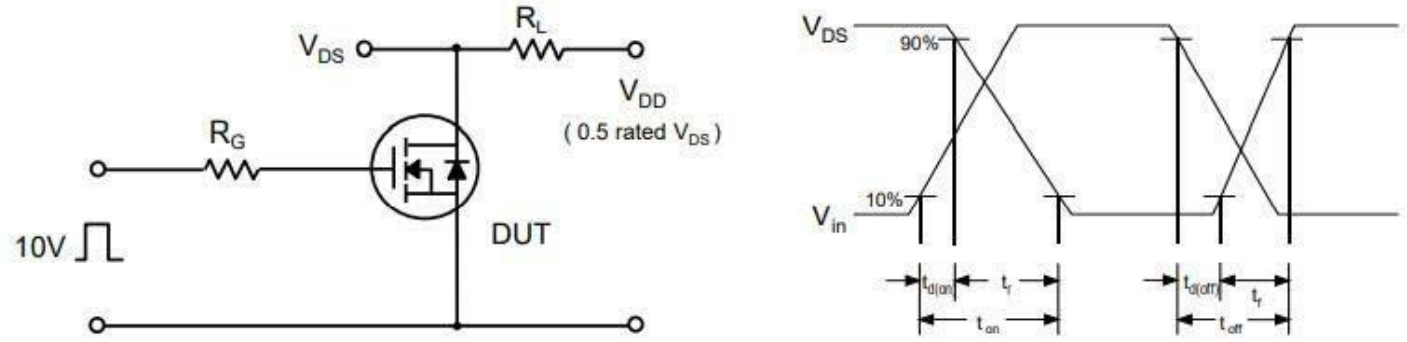


Figure 11. Resistive Switching Test Circuit & Waveforms

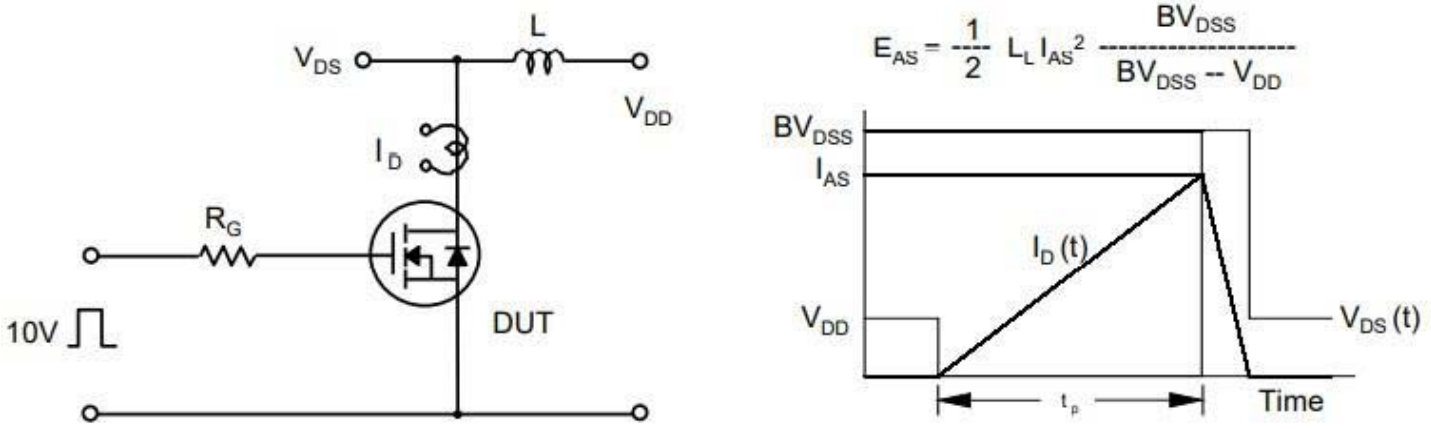


Figure 12. Unclamped Inductive Switching Test Circuit & Waveforms