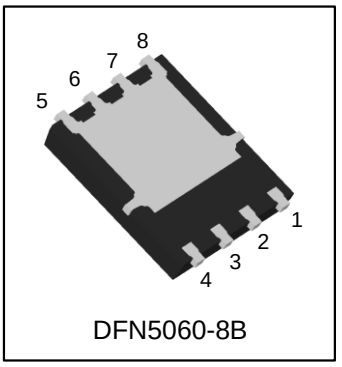
40V N-Channel Power MOSFET



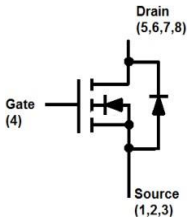
DFN5060-8B

1. FEATURES

- Advanced trench cell design
- Low Thermal Resistance
- High speed switch
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S-prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.

2. APPLICATIONS

- Power Tools
- DC-DC Converter
- Motor Control



3. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Shipping
S-LN7404DT3WG	LN7404	5000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter		Symbol	Limits	Unit
Drain-to-Source Voltage		VDS	40	V
Gate-to-Source Voltage		VGS	±20	V
Continuous Drain Current(Note 1)	TA=25℃	ID	24	A
	TA=75℃		21	
	TC=25℃		109	
	TC=75℃		95	
Pulsed Drain Current (Note 2)		IDM	96	A
Avalanche Current		IAS	35	A
Avalanche Energy(L=0.1mH)		EAS	61.25	mJ
Power Dissipation(Note 1)	TA=25℃	PD	2.5	W
	TC=25℃		62.5	
Operating Junction and Storage Temperature Range		Tj/Tstg	-55~+150	℃

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance,Junction-to-Ambient(Note 1)	RθJA	50	℃/W
Thermal Resistance,Junction-to-Ambient(Note 3)	RθJA	111	
Thermal Resistance,Junction-to-Case	RθJC	2	

1.Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu.

2.Pulse width limited by maximum junction temperature.

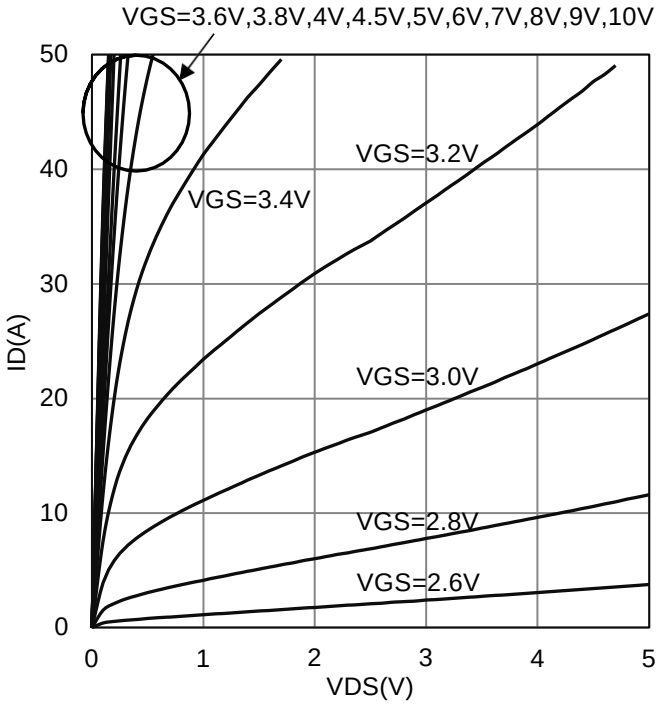
3.Surface mounted on FR4 board using the minimum recommended pad size.

6. ELECTRICAL CHARACTERISTICS (Ta= 25℃)

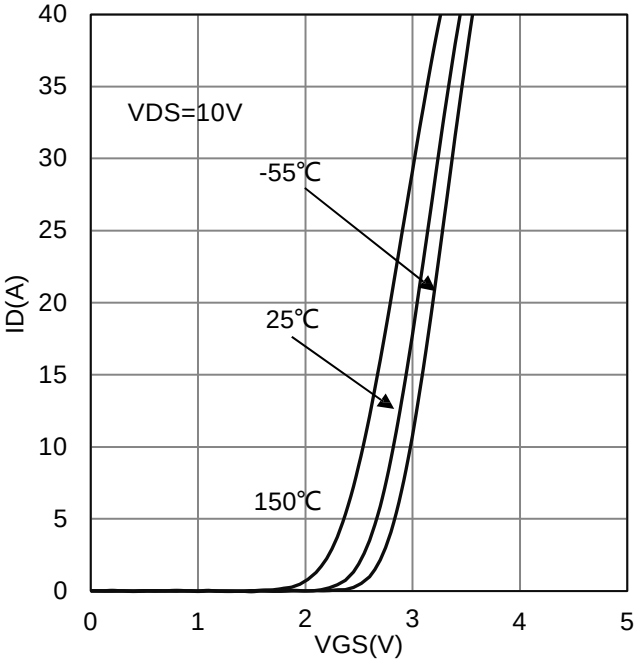
Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain–Source Breakdown Voltage (VGS = 0V, ID = 250μA)		V(BR)DSS	40	-	-	V
Gate Threshold Voltage (VDS = VGS , ID = 250μA)		VGS(th)	1	2	3	V
Gate Leakage Current (VDS = 0 V, VGS = ±20V)		IGSS	-	-	±100	nA
Zero Gate Voltage Drain Current (VDS = 32 V, VGS = 0 V)		IDSS	-	-	1	μA
Drain-Source On-Resistance(Note 4) (VGS = 10 V, ID = 15 A) (VGS = 4.5 V, ID = 15 A)		RDS(on)	 - -	 2 3.2	 3 4.3	mΩ
Diode Forward Voltage(Note 4) (IS = 1 A, VGS = 0 V)		VSD	-	0.7	1.3	V
Dynamic						
Total Gate Charge	(VDS = 20 V, VGS = 4.5 V,ID = 2 A)	Qg	-	23.6	-	nC
Gate-Source Charge		Qgs	-	5.5	-	
Gate-Drain Charge		Qgd	-	11.7	-	
Input Capacitance	(VDS = 15 V, VGS = 0 V, f = 1 MHz)	Ciss	-	2478	-	pF
Output Capacitance		Coss	-	1387	-	
Reverse Transfer Capacitance		Crss	-	146	-	
Turn-On Delay Time	(VDS = 20 V, RL = 1.3 Ω,ID = 2 A,VGEN = 10 V, RGEN = 6 Ω)	td(on)	-	13	-	ns
Rise Time		tr	-	18	-	
Turn-Off Delay Time		td(off)	-	68	-	
Fall Time		tf	-	37	-	

4.Pulse test: PW≤ 300μs duty cycle ≤ 2%.

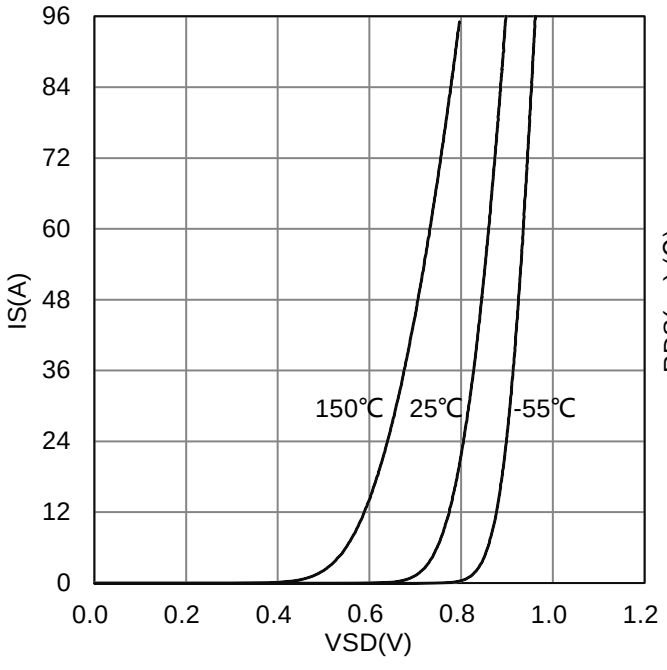
7 ELECTRICAL CHARACTERISTICS CURVES



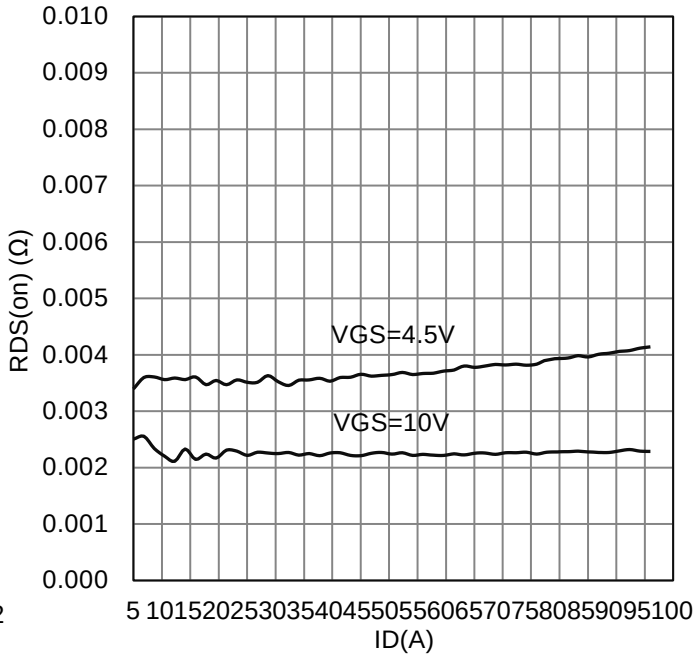
ID vs. VDS



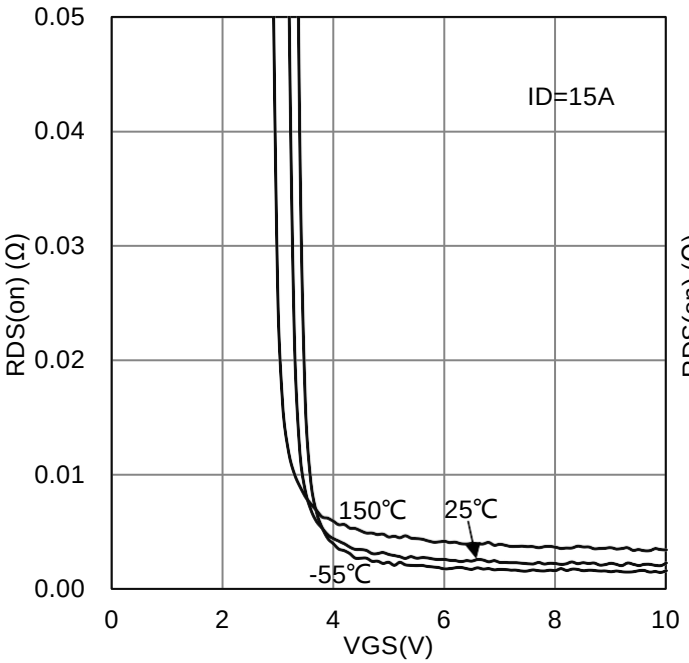
ID vs. VGS



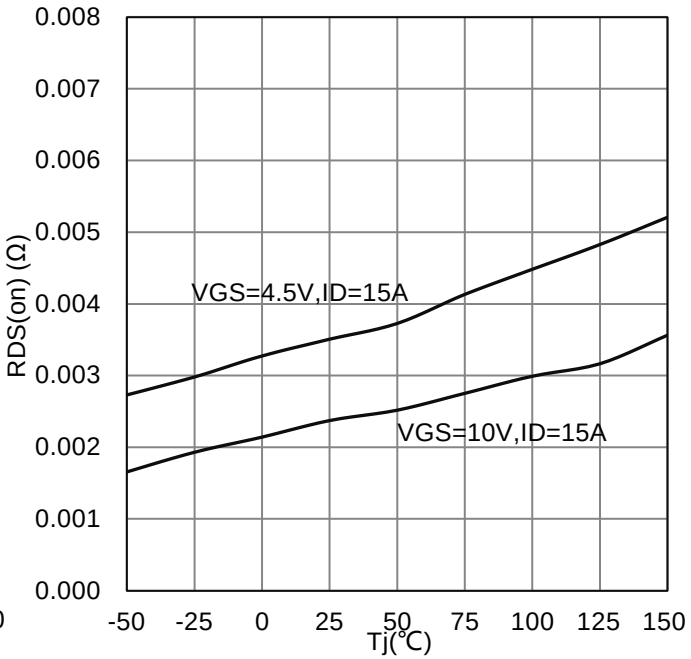
IS vs. VSD



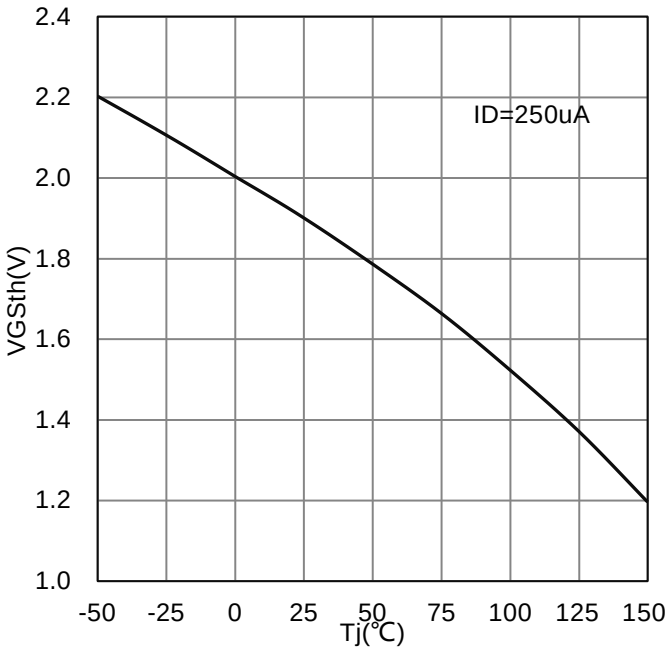
RDS(on) vs. ID



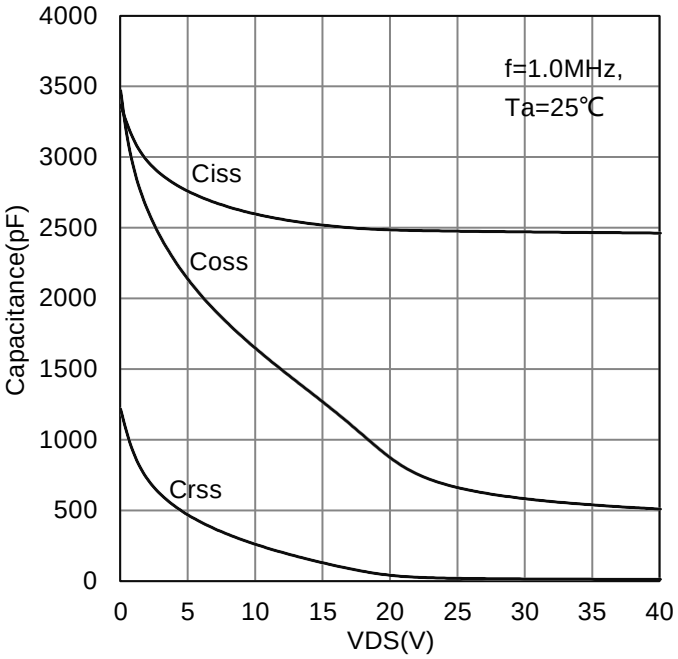
RDS(on) vs. VGS



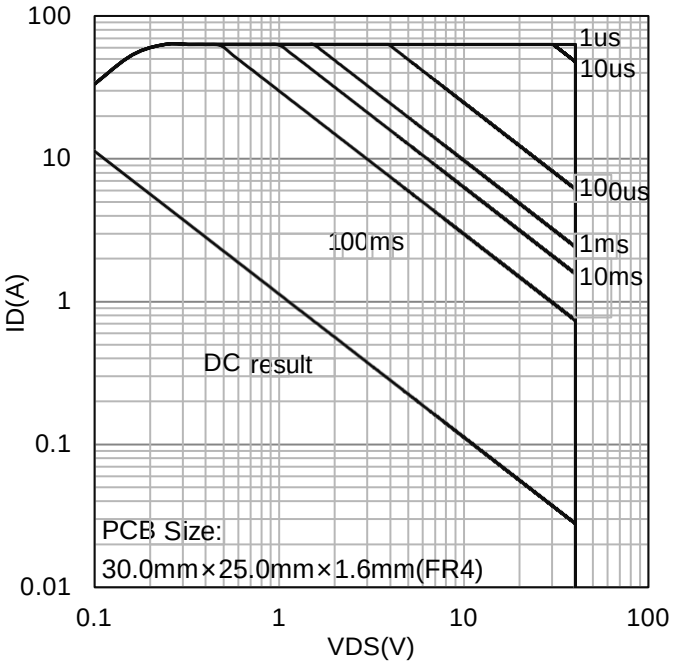
RDS(on) vs. Tj



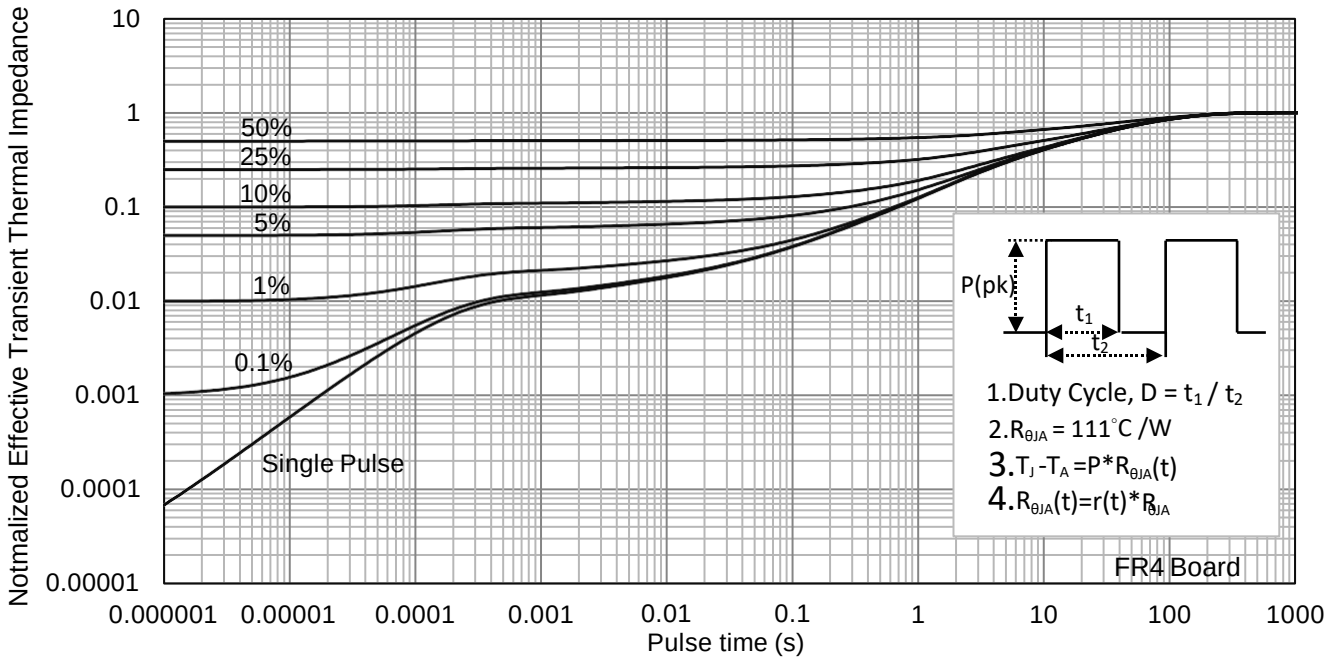
VGSth vs. Tj



Capacitance



Safe Operating Area



Thermal Response

8.OUTLINE AND DIMENSIONS

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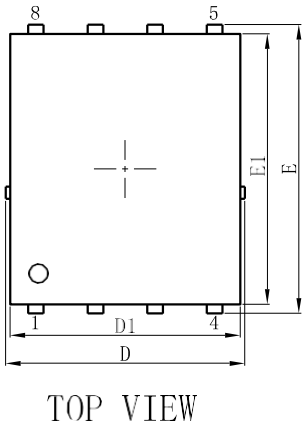
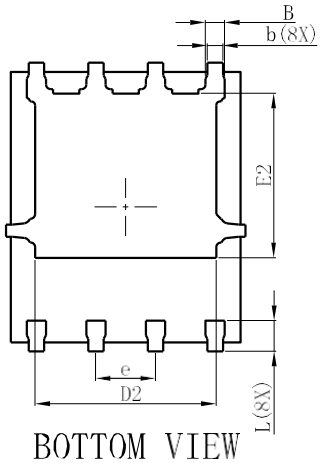
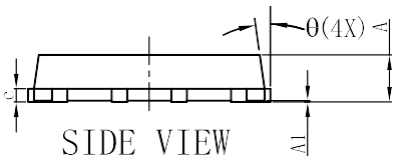




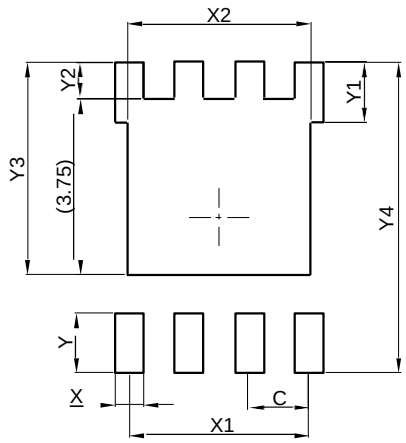
DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0°	-	12°
All Dimensions in mm			



GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9.SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61